DATA MODUL

SPECIFICATION

ED013TC1

1.27”, 128x256, SPI

Version: 1.0
Date: 30.10.2017

Note: This specification is subject to change without prior notice

www.data-modul.com

Version: 1.0

TECHNICAL SPECIFICATION

MODEL NO: ED013TC1

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

■E Ink's Confirmation

Approved By 李紹燦

Confirmed By 吳漢銳

Prepared By 吳岱南

Revision History

Rev.	Issued Date	Revised Contents
0.1	Feb 1, 2016	Preliminary
0.2	Aug 5, 2016	Add Ch14~17. Update Module Weight & Features. Update Optical characteristics, Reliability test, Input/ Output Interface, Electrical Characteristics, and Power Sequence. Update Mechanical Drawing of EPD Module, Packing.
0.3	May 17, 2017	Modify FPC Shape on Ch4, 5-3, 11, 13. Outline Dimension modified.
1.0	Oct 30, 2017	Modify the setting of, 17-1) R00H (PSR): Panel setting Register 17-22) R61H (TRES) Resolution Setting

TECHNICAL SPECIFICATION

CONTENTS

1. General Description

ED013TC1 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 1.27” active area with 128x256 pixels, the display is capable to display images at 2 gray levels (1 bit) depending on the display controller and the associated waveform file it used.

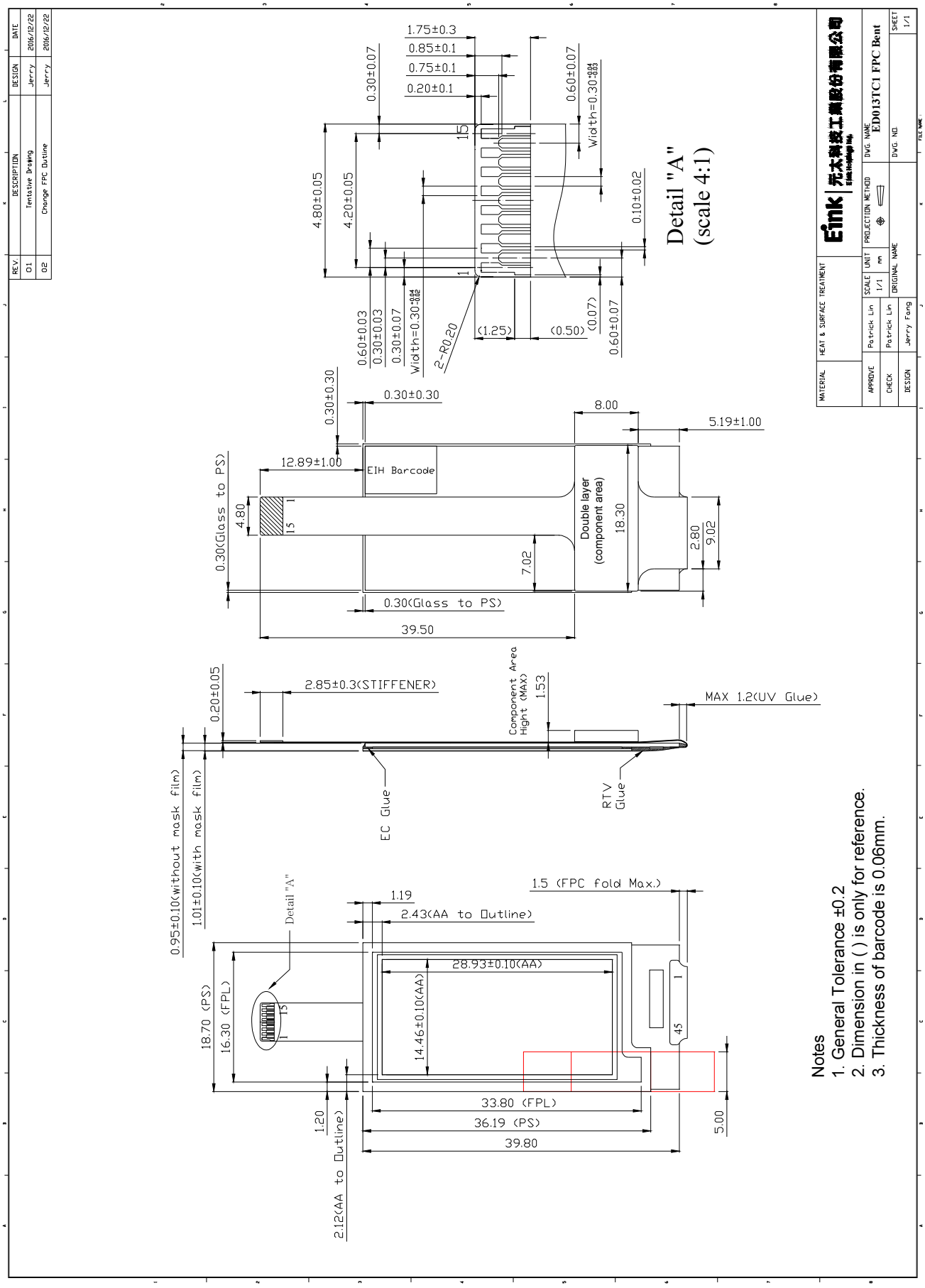
2. Features

- High contrast reflective/electrophoretic technology
- 128x256 resolution
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- SPI interface to EPD display
- Share with system flash, 20Kbyte (per waveform mode) need for display waveform LUT(Look-Up Table) and support display modes

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.27	Inch	
Display Resolution	128 (H) × 256(V)	Pixel	
Active Area	14.464 × 28.928	mm	
Pixel Pitch	0.113(H) × 0.113(V)	mm	
Pixel Configuration	Rectangle		
Outline Dimension	18.7(H) × 39.8(V) × 0.95(D) (w/o MF) 18.7(H) × 39.8(V) × 1.01(D) (w/ MF)	mm	Display Only
Module Weight	1.55±0.16	g	Without mask film
Number of Gray	2		
Display operating mode	Reflective mode		

4. Mechanical Drawing of EPD Module



5. Input/ Output Interface

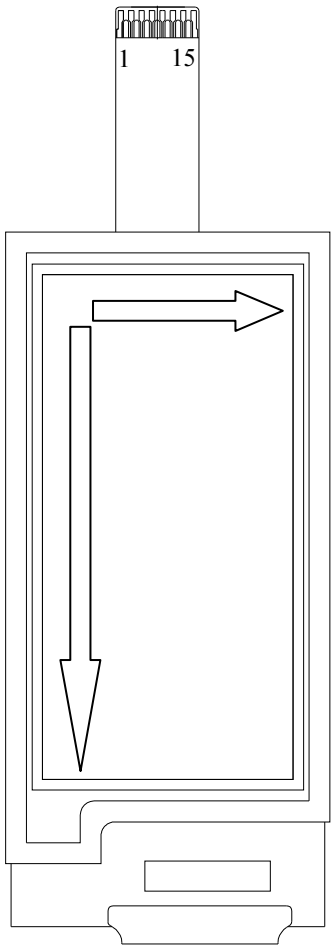
5-1) Connector type: FH35C-15S-0.3SHW(50)

5-2) Pin Assignment

Pin #	Signal	Description	Remark
1	NC	NC	
2	VSS	Ground	
3	VDD	Power Supply	
4	SDA	Serial data pin (SPI)	
5	SCL	Serial clock pin (SPI)	
6	CSB	Chip Select input pin	
7	DC	Data /Command control pin	
8	RST_N	Reset	
9	BUSY_N	Busy state output pin	
10	BS	Bus selection pin;L: 4-wire H: 3-wire	
11	TSDA	I2C Interface to digital temperature sensor	Note 1
12	TSCL	I2C Interface to digital temperature sensor	Note 1
13	NC	NC	
14	NC	NC	
15	NC	NC	

Note 1 : Option for external temperature sensor.

5-3) Panel Scan Direction



6. Electrical Characteristics

6-1) Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +6	V	--
Operating Temp. Range	TOTR	0 to +50	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

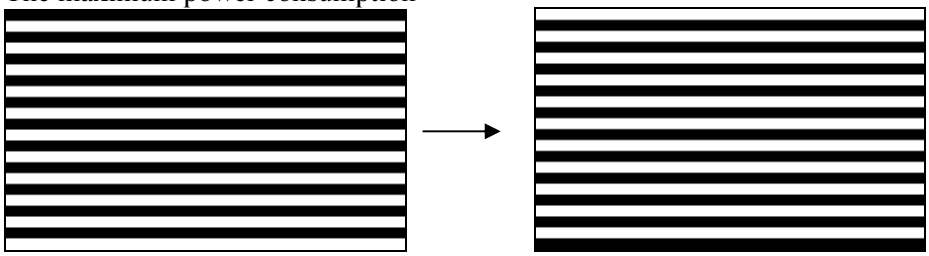
6-2) Panel DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	VSS		-	0	-	V
Logic voltage supply	VDD		2.3	3.3	3.6	V
	IVDD	VDD=3.3V	-	7.3	14.1	mA
Typical power panel	Ptyp		-	24	51	mW
Standby power panel	Pstby		-	-	0.1	mW

- The maximum power consumption is measured with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 7-1)
- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Note 7-2)
- The standby power is the consumed power when the panel controller is in standby mode.
- .

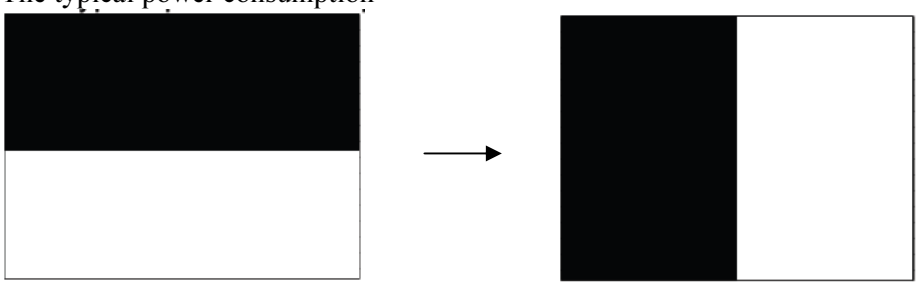
Note7-1

The maximum power consumption



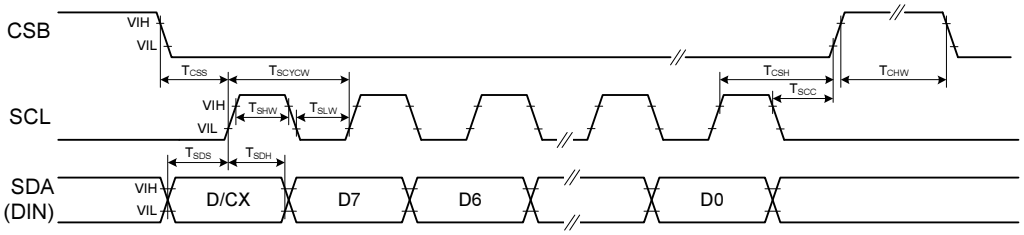
Note7-2

The typical power consumption

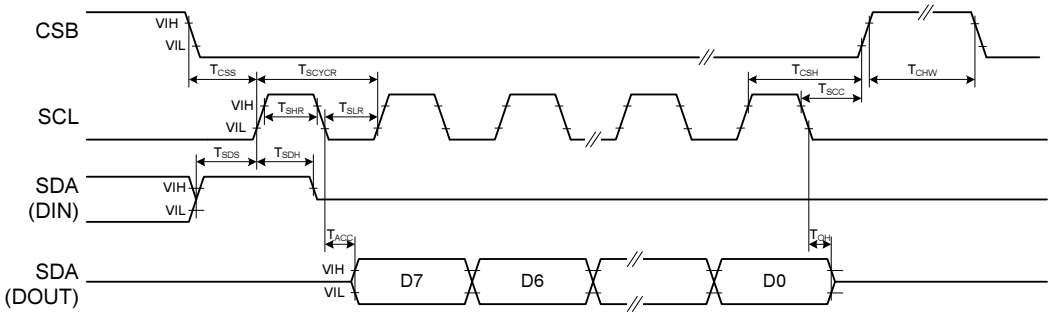


6-3) Panel AC characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SERIAL COMMUNICATION						
CSB	t_{CSS}	Chip select setup time	60			ns
	t_{CSH}	Chip select hold time	65			ns
	t_{SCC}	Chip select setup time	20			ns
	t_{CHW}	Chip select setup time	40			ns
SCL	t_{SCYCW}	Serial clock cycle (Write)	100			ns
	T_{SHW}	SCL “H” pulse width (Write)	35			ns
	t_{SLW}	SCL “L” pulse width (Write)	35			ns
	t_{SCYCR}	Serial clock cycle (Read)	150			ns
	T_{SHR}	SCL “H” pulse width (Read)	60			ns
	t_{SLR}	SCL “L” pulse width (Read)	60			ns
SDA (DIN) (DOUT)	t_{SDS}	Data setup time	30			ns
	t_{SDH}	Data hold time	30			ns
	t_{ACC}	Access time	10			ns
	t_{OH}	Output disable time	15			ns



3 pin serial interface characteristics (write mode)

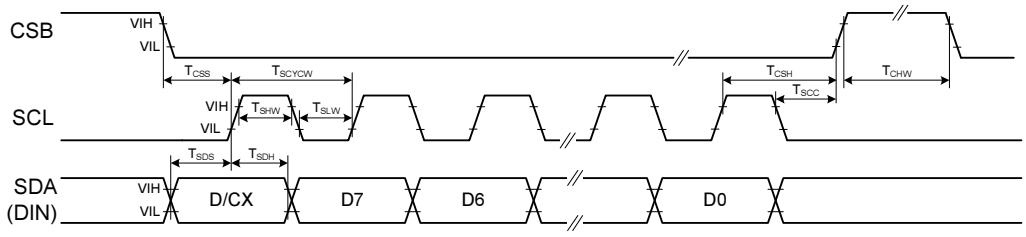


3 pin serial interface characteristics (read mode)

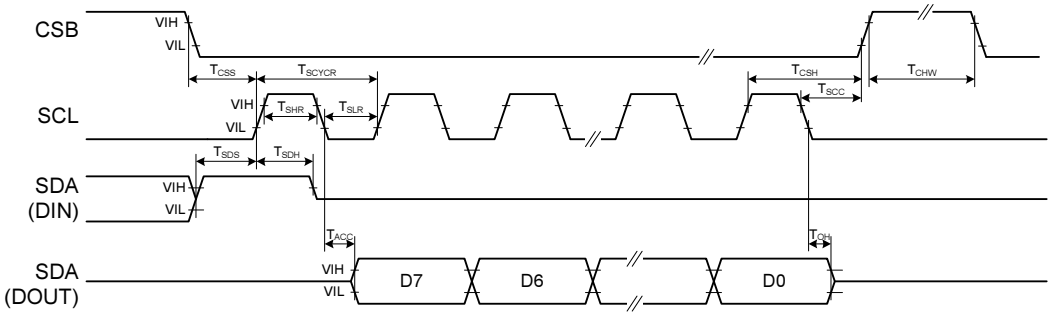
6-4) Controller Timing

SPI COMMAND

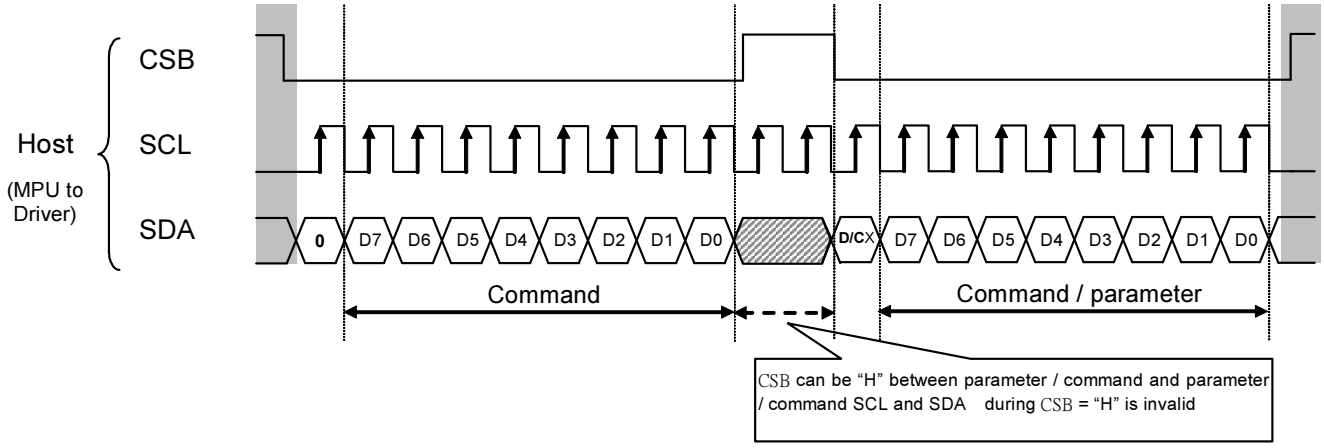
3 wire SPI format



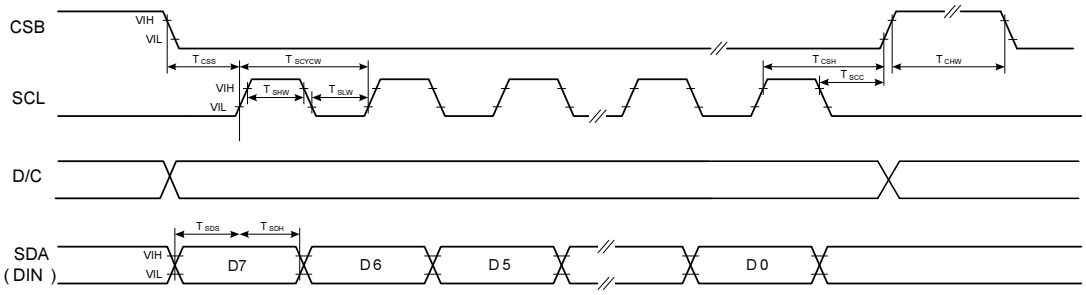
3 pin serial interface characteristics (write mode)



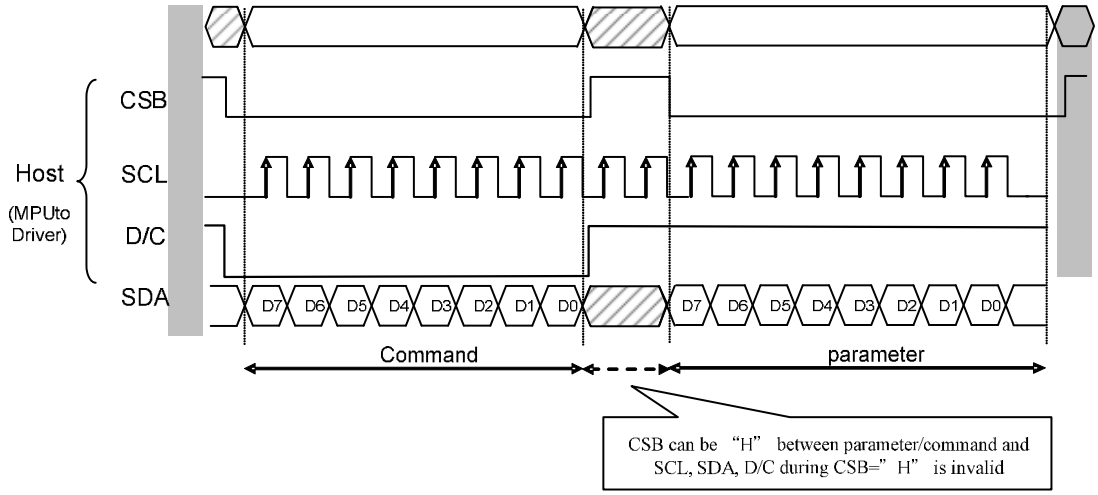
3 pin serial interface characteristics (read mode)



4 wire SPI format

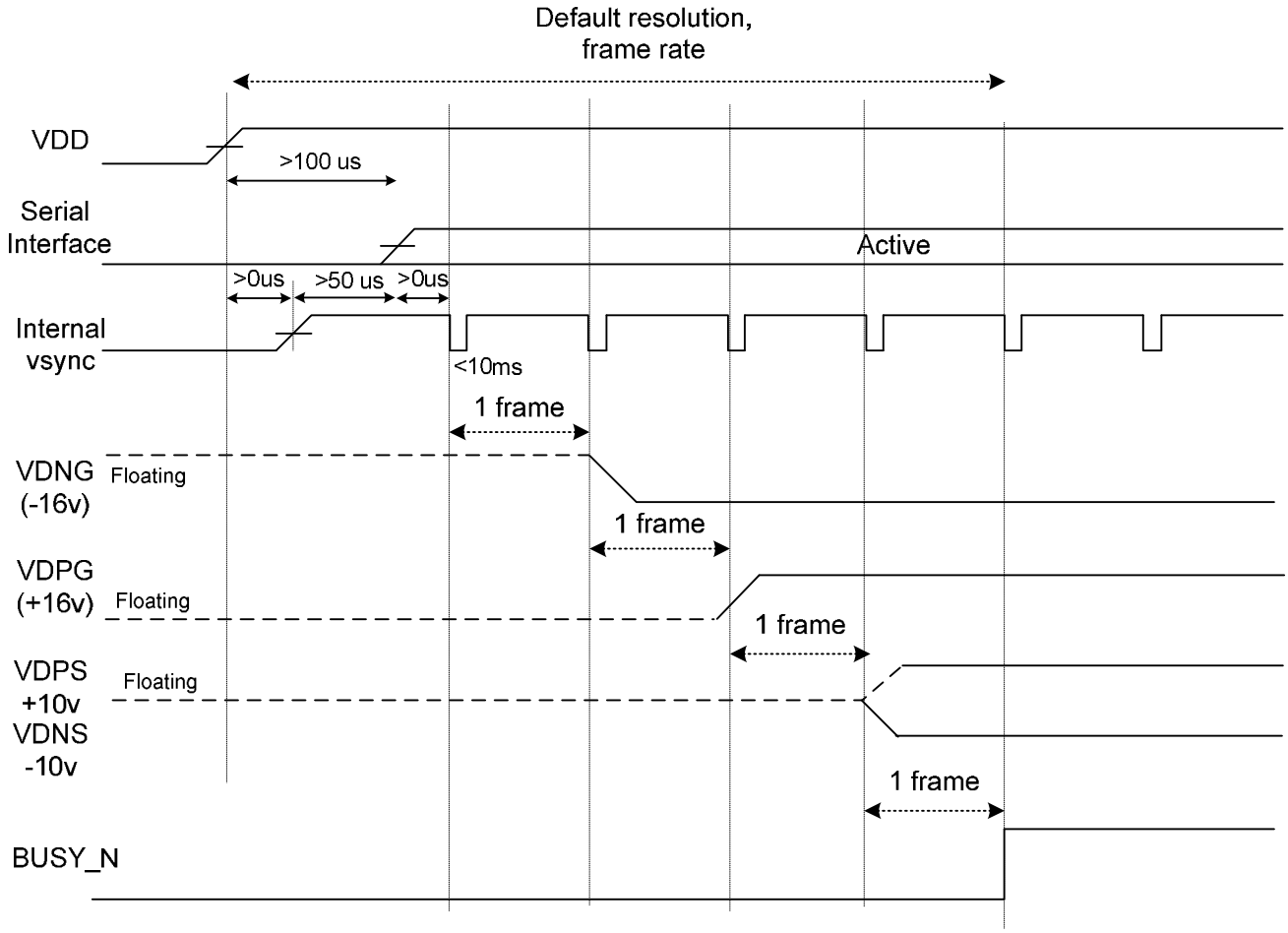


4 pin serial interface characteristics

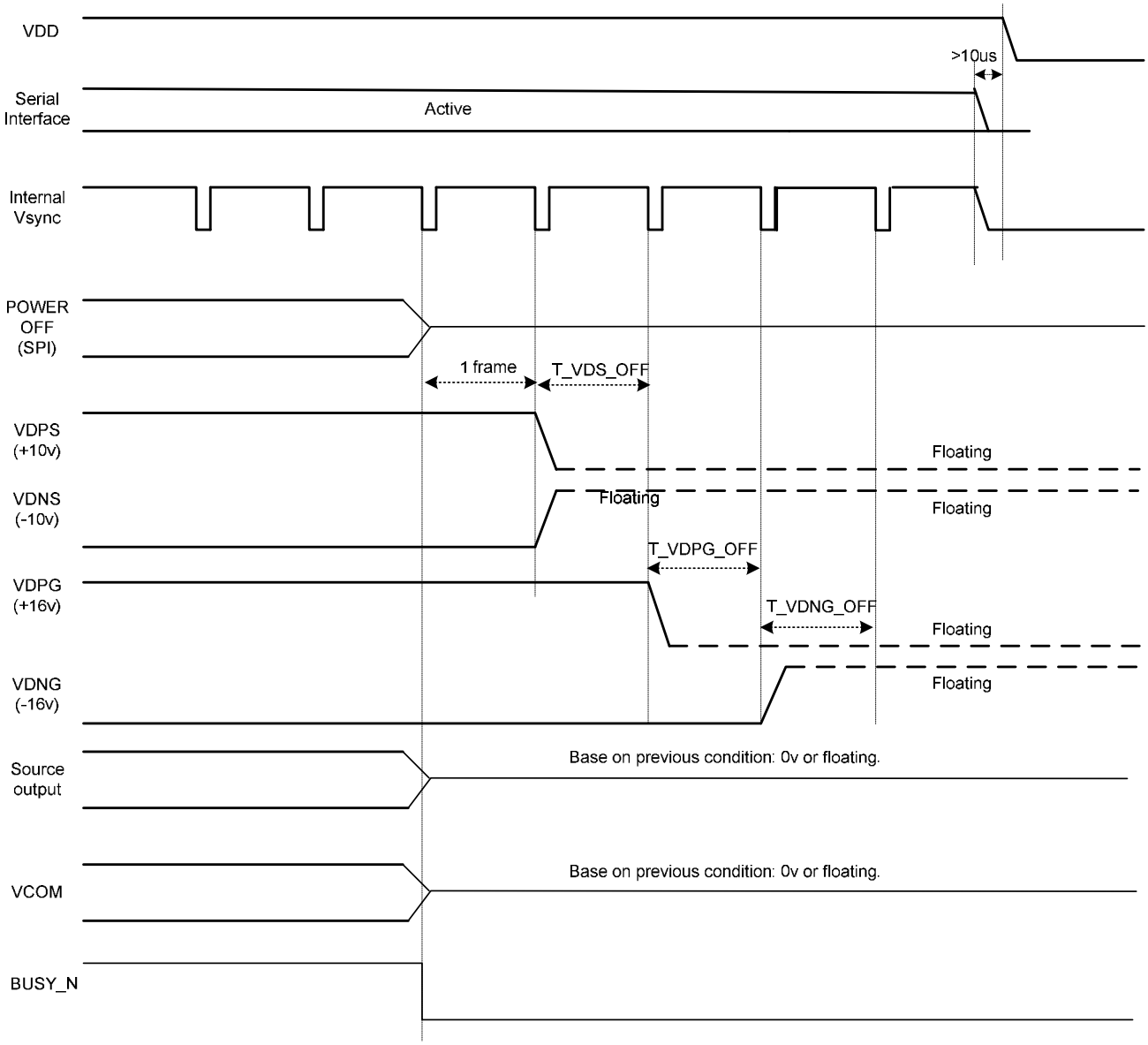


7. Power Sequence

POWER ON



POWER OFF



8. Optical Characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

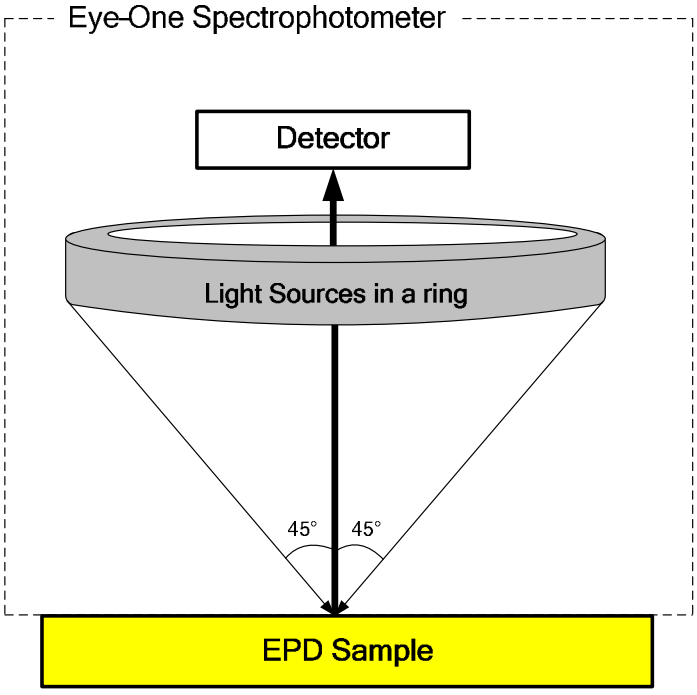
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 8-1
CR	Contrast Ratio	-	9	12	-		-

WS: White state , DS: Dark state

Note 8-1: Luminance meter : Eye – One Pro Spectrophotometer.

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl / Rd



8-3) Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \quad x \quad (L_{center} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements and Remark

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.
REMARK
All the specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any post-assembly operation.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains preliminary product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

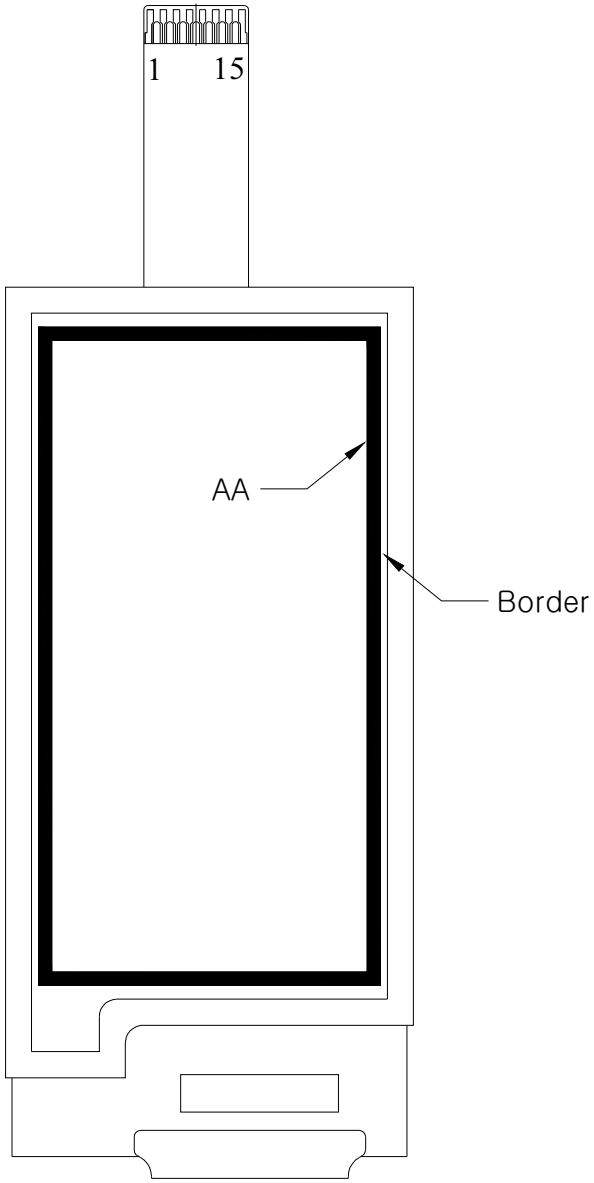
10. Reliability Test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=40% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
6	High Temperature, High- Humidity Storage	T = +60℃, RH=80% for 240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ Test in white pattern	IEC60 068-2-5Sa	
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	
10	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3 edges, 6 faces One drop for each.	Full packed for shipment	
11	Electrostatic Effect (non-operating)	(Machine model)+/− 250V 0Ω, 200pF	IEC 62179, IEC 62180	
12	Stylus Tapping	POLYACETAL Pen: Top R:0.8mm Load: 300gf Speed: 2 times/sec Total 13,500times,		

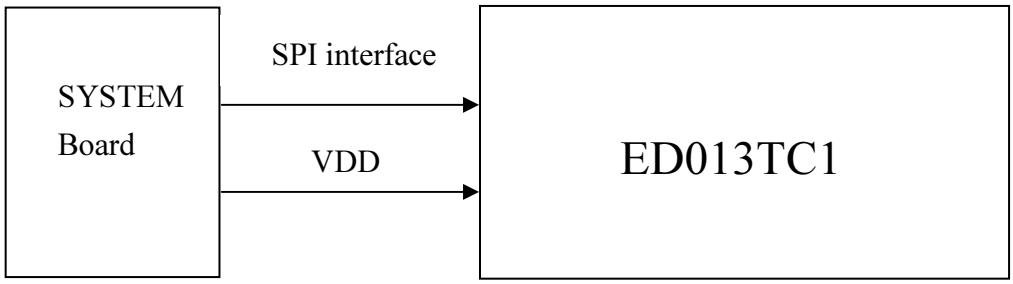
Actual EMC level to be measured on customer application
Note: The protective film must be removed before temperature test.

< Criteria >
In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

11. Border Definition

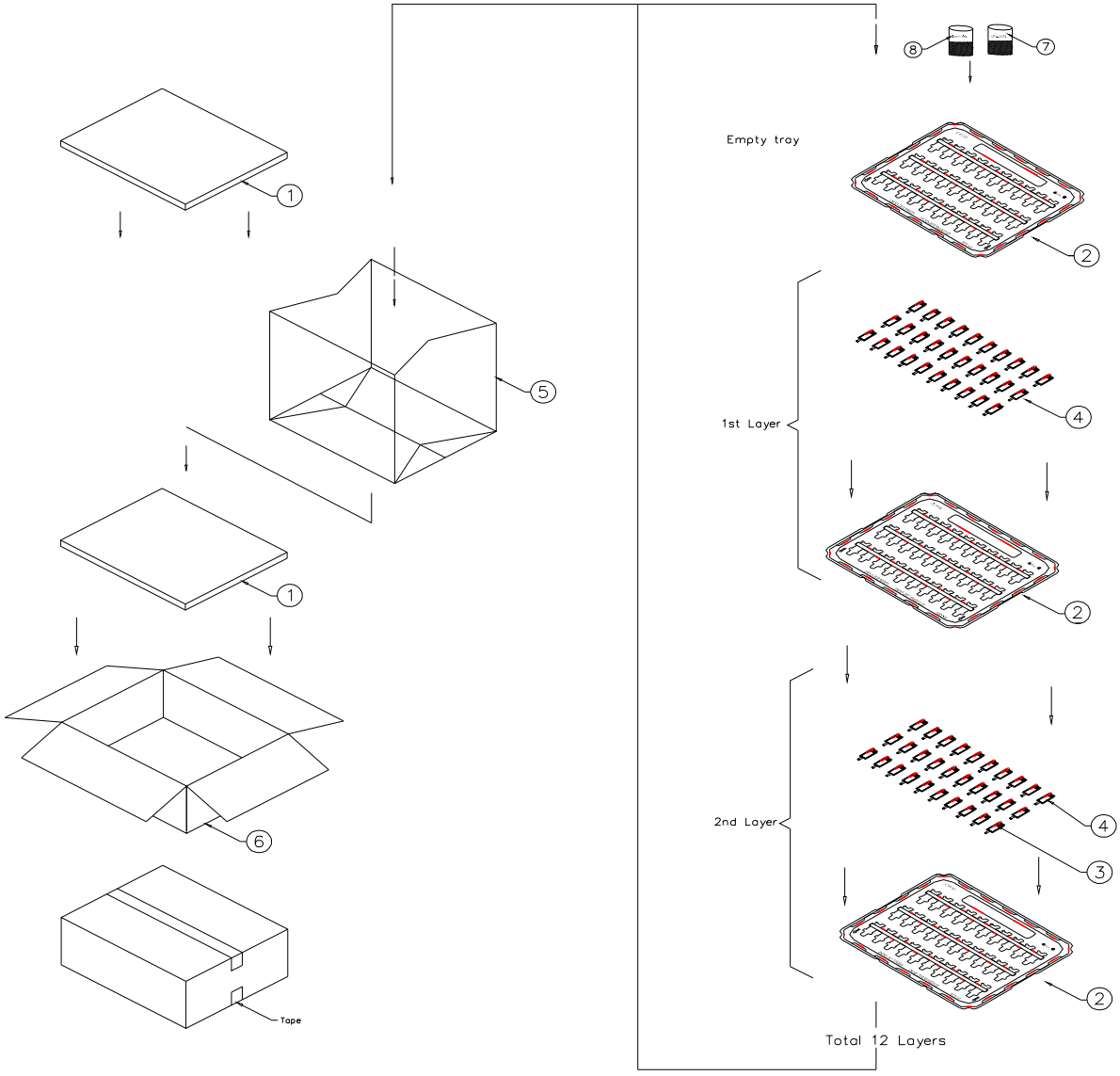


12. Block Diagram



13. Packing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Jerry	'16.12.22



NOTE:

1. One layer include:
   30 pcs module & 1 piece of tray.
2. Q'TY: 360 pcs panel/carton.
3. Dimension: 445*365*170mm
4. Weight: 3.4KG
5. Make sure tray stacked with 0 degree rotation.

ITEM	DESCRIPTION	QTY	REMARK
8	30g加厚積合紙活礦乾燥劑73*95mm	2	
7	防鏽劑(保護容積25L)	3	
6	CARTON INTERNAL	1	
5	摺口袋450*380*580mm	1	抗靜電
4	ED013TC1	360	
3	Peeling tape	360	抗靜電
2	TRAY	13	抗靜電
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ±5.0mm ANGLE ROUGHNESS	REMARK	E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.			
APPROVE	Patrick Lin	'16.12.22	SCALE 1:1	UNIT mm	SHEET 1 OF 1	DWG.TITLE ED013TC1 PACKING Dim
CHECK	Patrick Lin	'16.12.22	MTL.NO.	DWG.NO.	REV. 01	A4 SIZE
DESIGN	Jerry Fang	'16.12.22				

14. Reference circuit

Figure. ED013TC1 Reference Circuit

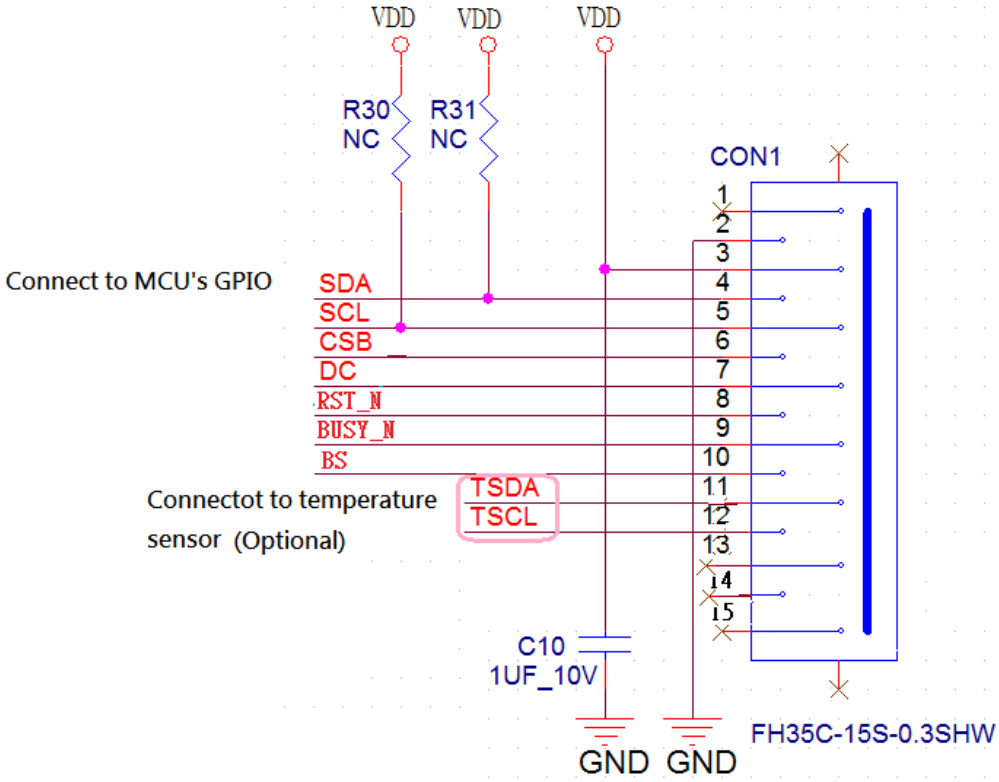
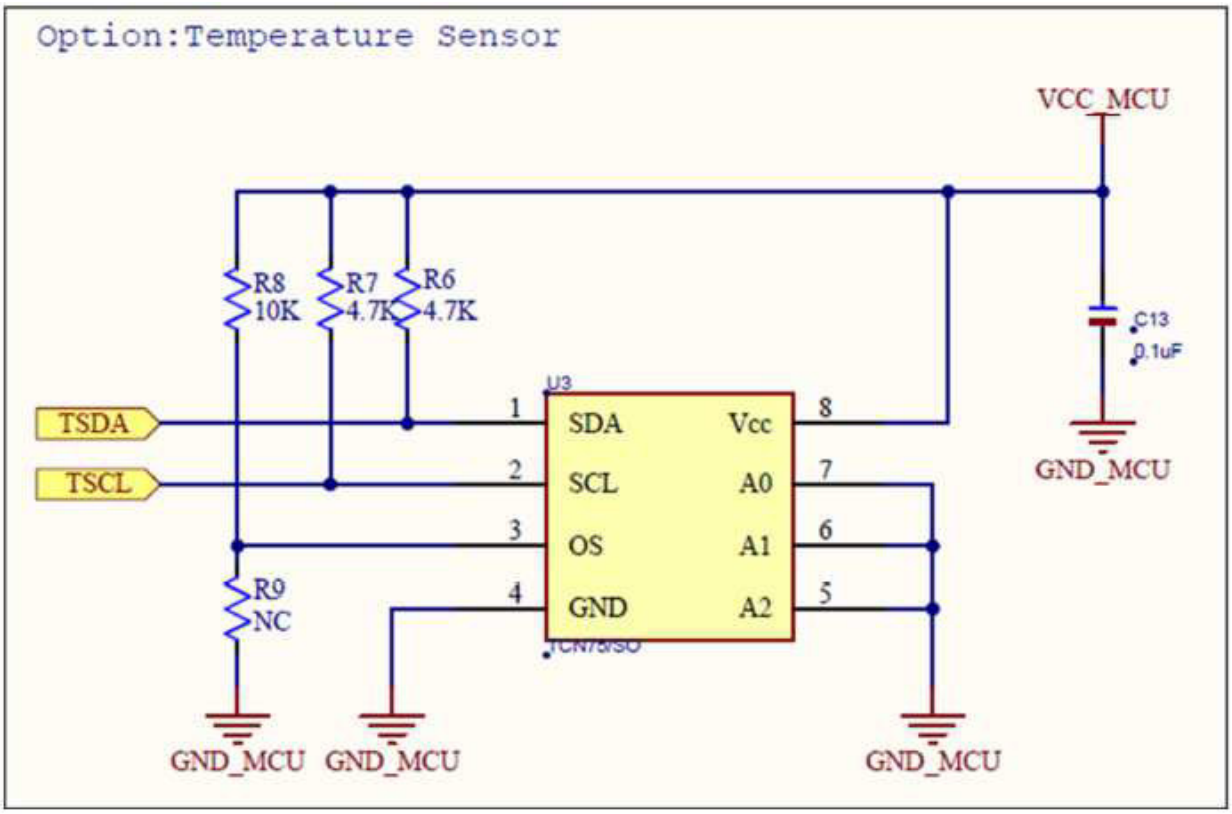
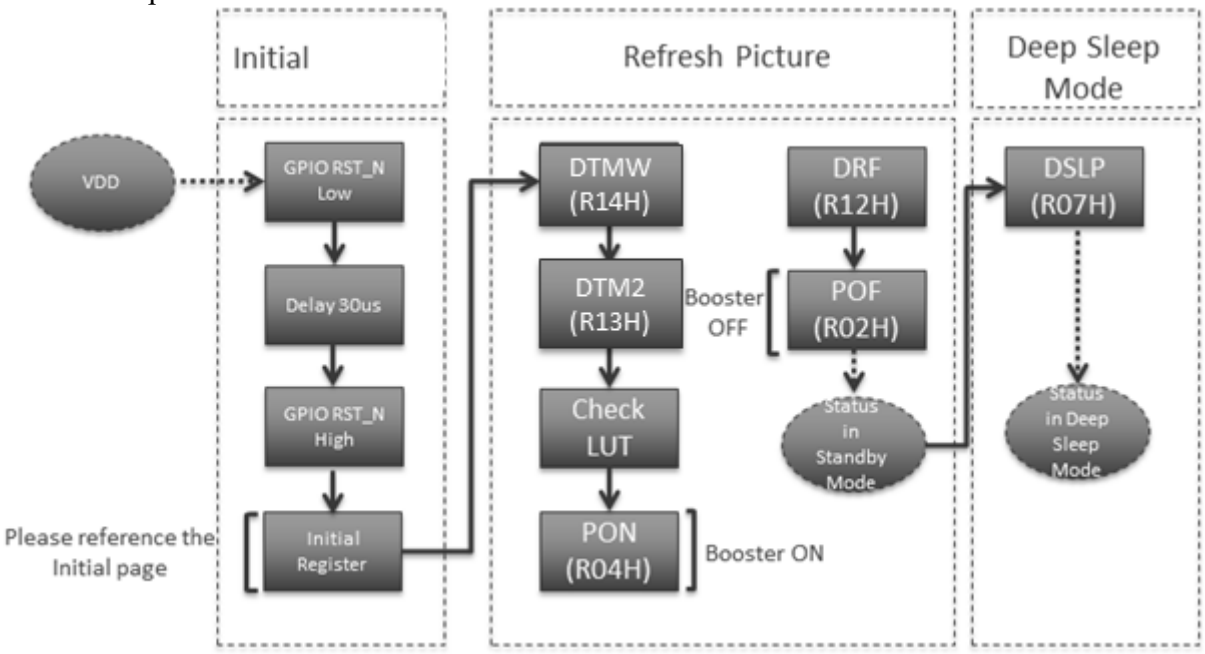


Figure. Temperature Sensor Circuit (Optional)

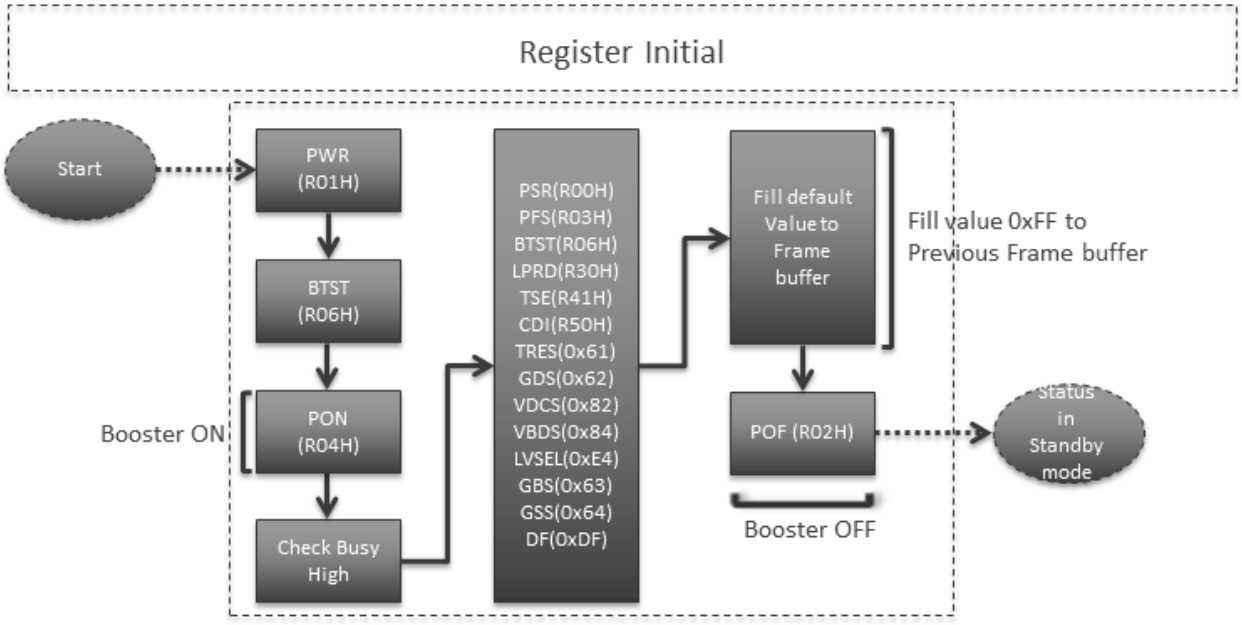


15. Software Programming Guide

This section describes the image update flow for the ED013TC1. After the system MCU sends a 1-bit image to the driver IC, the BUSY signal from the panel should be monitored and used to indicate the completion of the update.



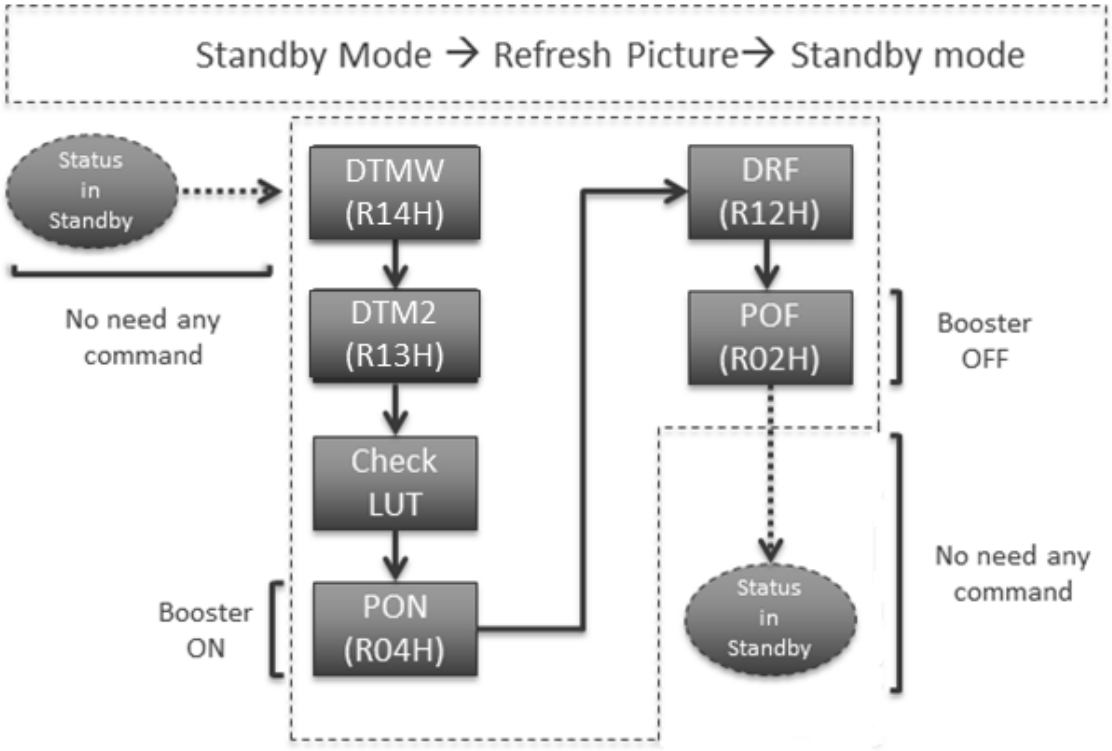
- Please reference Registers initial flow to initial registers
- DTM1 and DTM2 is for 2 Bpp image data
- DTM3 and DTM4 is for 1 Bpp image data
- DTM1 and DTM3 is previous frame buffer
- DTM2 and DTM4 is current frame buffer



- In frist time power on, the previous Frame buffer data is random, so we need initial buffer data to white(0xFF is mean white)
- Please reference the sample code to set all registers.

16. User Mode Flow Chart

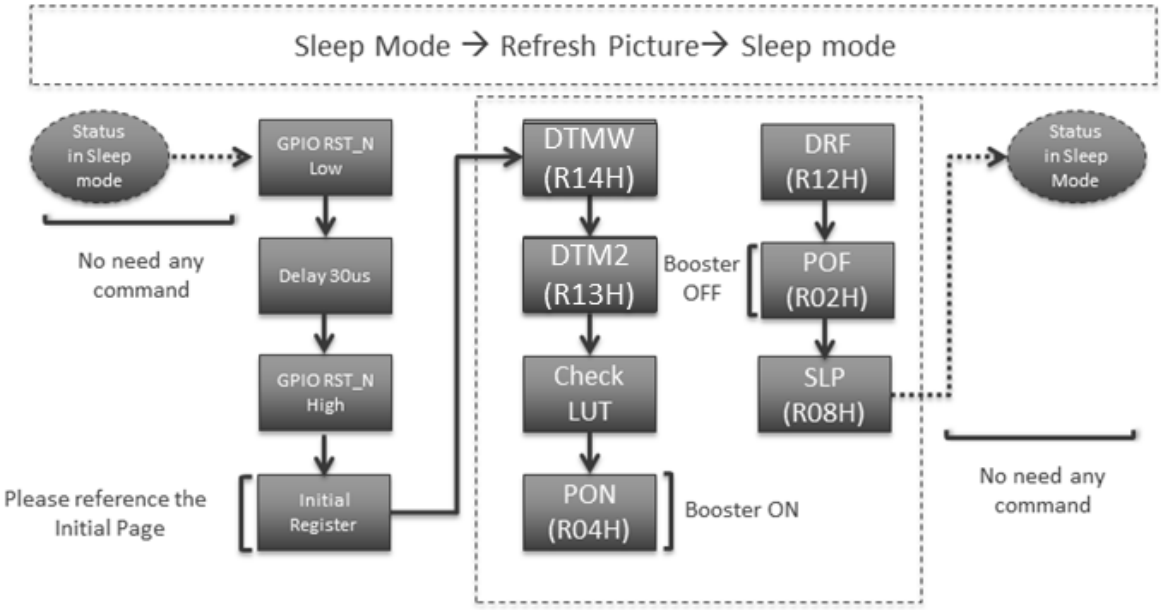
16-1)Standby Mode



Item	Character
VDDDO	1.8V
Booster	OFF
Keep Frame Buffer	Yes
Keep Registers Setting	Yes

Note: Please reference Initial Registers page for initial registers stage

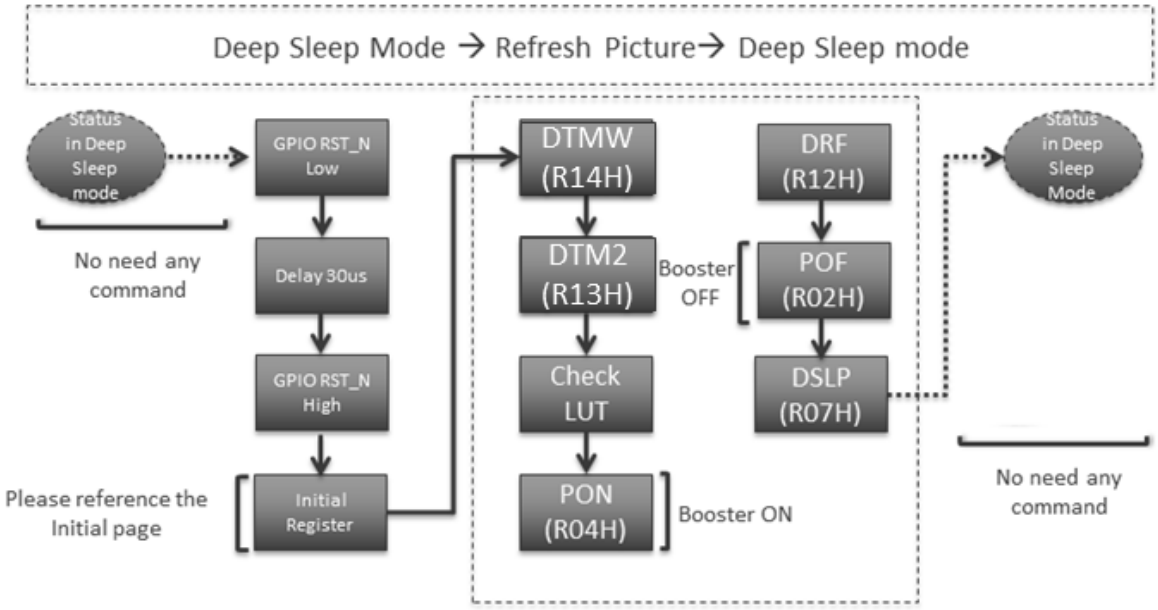
16-2) Sleep Mode



Item	Character
VDDDO	1.0V
Booster	OFF
Keep Frame Buffer	Yes
Keep Registers Setting	Not Guarantee

Note: Please reference Initial Registers page for initial registers stage

16-3) Deep Sleep Mode

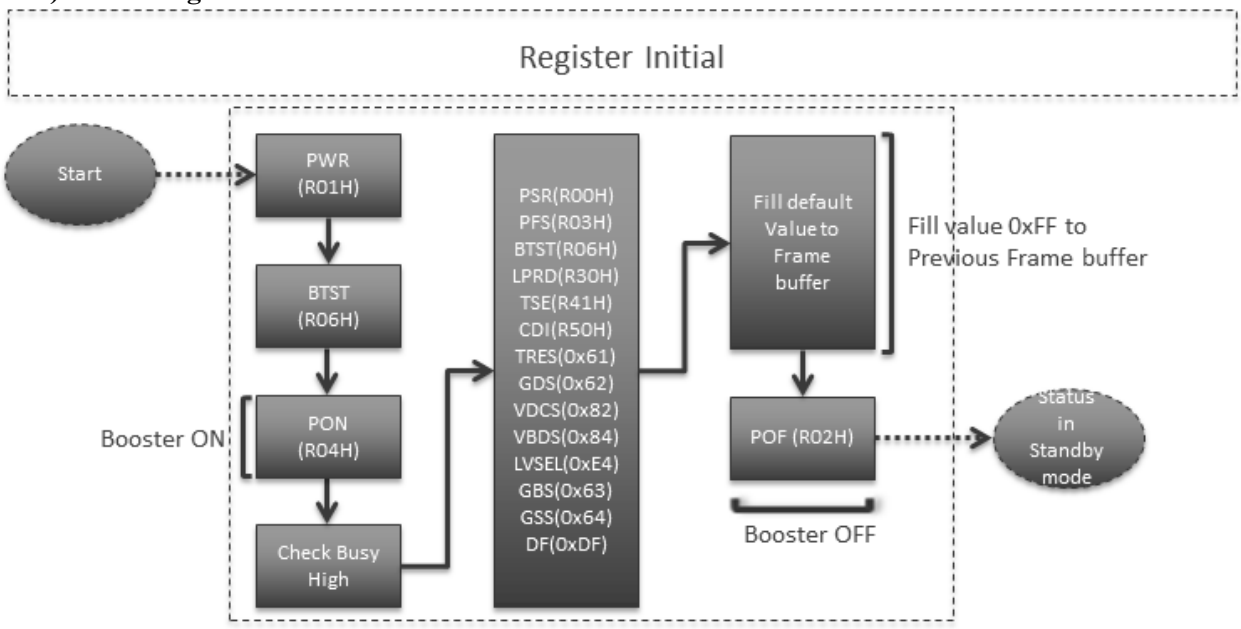


Item	Character
VDDDO	0.0V
Booster	Off
Keep Frame Buffer	No
Keep Registers Setting	No

Note:

1. In “Deep Sleep Mode”, the control signals are recommended tied to 0V and RST_N is released to floating
2. Base IC Die must be keep away from light which causes photoelectric effect to make internal nodes unstable
3. Please reference Initial Registers page for initial registers stage

16-4) Initial Registers



Note:

1. In frist time power on, the previous Frame buffer data is random, so we need initial buffer data to white(0xFF is mean white)
2. Please reference the sample code to setall registers.

17. Command Table

Register Definition

17-1) R00H (PSR): Panel setting Register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	W	1	0	0	-	0	0	SHL	SHD_N	RST_N
	W	REG_EN	1	-	-	-	-	1	1	0

NOTE: "-" Don't care, can be set to VDD or GND level

SHL: 0: Shift left.

1: Shift right. (default)

SDMD	SHL	Source order (128 channels)	Source order (Reduced: S63~S60)
0: Edge start	0: Shift right	S127 → … → S64 → S63 → … → S0	S127 → … → S64 → S59 → … → S0
0: Edge start	1: Shift left	S0 → … → S63 → S64 → … → S127	S0 → … → S59 → S64 → … → S127
1: Center start	0: Shift right	S63 → … → S0 → S127 → … → S64	S59 → … → S0 → S127 → … → S64
1: Center start	1: Shift left	S64 → … → S127 → S0 → … → S63	S64 → … → S127 → S0 → … → S59

SHD_N: Booster Shutdown

0: Booster shutdown and register data kept.

1: No booster shutdown (default)

RST_N: Soft Reset.

0: Assert reset function : Booster OFF and Register data reset to it default value.

1: No effect (default)

REG_EN: LUT selection

0: Using LUT from OTP (default)

1: Using LUT from internal register

17-2) R01H (PWR): Power setting Register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	W	1	**-**	**-**	-	-	-	-	VS_EN	VG_EN
	W	1	**-**	**-**	**-**	**-**	**-**	0	0	0
	W	1	**-**	**-**	0	1	1	1	0	0
	W	1	**-**	**-**	0	1	1	1	0	0
	W	1	**-**	**-**	0	0	1	0	0	0

NOTE: "-" Don't care, can be set to VDD or GND level

VS_EN: Source power selection

0 : External source power from VDH/VDL pins

1 : Internal DC/DC function for generating VDH/VDL

VG_EN: Gate power selection

0 : External gate power from VGH/VGL pins

1 : Internal DC/DC function for generating VGH/VGL

17-3) R02H (POF): Power OFF Command

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

After the Power Off command, driver will power off based on the Power Off Sequence, BUSY_N will become "0". This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

SD output and Vcom will base on previous condition. It may have 2 conditions: 0V or floating.

This command can be active only when BUSY_N = "1".

17-4) R03H (PFS): Power off sequence setting Register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**
	W	1	**-**	**-**	T_VDS_OFF[1:0]		**-**		**-**	

NOTE: "-" Don't care, can be set to VDD or GND level

T_VDS_OFF[1:0]: Power OFF Sequence of VDPS and VDNS.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

This command can be active only when BUSY_N = "1".

17-5) R04H (PON): Power ON Command

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	W	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**

After the Power ON command, the driver will be powered ON following the Power ON Sequence. After the Power ON command and all power sequence are ready, the BUSY_N signal will become "1". Refer to the Power ON Sequence section.

17-6) R06h (BTST): Booster Soft Start

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	W	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**
	W	1	BTPHA7	BTPHA6	BTPHA5	BTPHA4	BTPHA3	BTPHA2	BTPHA1	BTPHA0
	W	1	BTPHB7	BTPHB6	BTPHB5	BTPHB4	BTPHB3	BTPHB2	BTPHB1	BTPHB0
	W	1	-	-	BTPHA5	BTPHC4	BTPHC3	BTPHC2	BTPHC1	BTPHC0

NOTE: "-" Don't care, can be set to VDD or GND level

BTPHA[7:6]: Soft start period of phase A

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3] : Driving strength of phase A

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4

100b: strength 5 (strongest) 101b: strength 6 110b: strength 7 111b: strength 8

BTPHA[2:0] : Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS

100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

BTPHB[7:6] : Soft start period of phase B

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3] : Driving strength of phase B

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4

100b: strength 5 (strongest) 101b: strength 6 110b: strength 7 111b: strength 8

BTPHB[2:0] : Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

BTPHC[5:3] : Driving strength of phase C

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4

100b: strength 5 (strongest) 101b: strength 6 110b: strength 7 111b: strength 8

BTPHC[2:0] : Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

17-7) R07H (DSLP): Deep sleep

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep sleep	W	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
	W	1	1	0	1	0	0	1	0	1

This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion.

The only one parameter is a check code, the command would be executed if check code is A5h.

17-8) R08H (SLP): sleep

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
sleep	W	0	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
	W	1	1	0	1	0	0	1	0	1

This command makes the chip enter the sleep mode. The sleep mode could return to stand-by mode by hardware reset assertion.

The only one parameter is a check code, the command would be executed if check code is A5h.

17-9) R10H (DTM1): Data Start Transmission 1

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	W	0	0	0	0	1	0	0	0	0
	W	1	Pixel0[1:0]		Pixel1[1:0]		Pixel2[1:0]-		Pixel3[1:0]	
	W	1	…		…		…		…	
	W	1	Pixel(N-4)[1:0]		Pixel(N-3)[1:0]		Pixel(N-2)[1:0]		Pixel(N-1)[1:0]	

This command indicates that user starts to transmit data. Then write to old SRAM**:**

	Source Driver Output	
	DDX=1(Default)	DDX=0
Pixel[1:0]	LUT	LUT
00	Black	White
01	-	-
10	-	-
11	White	Black

17-10) R12H (DRF): Display Refresh

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
(8 byte command)	W	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**
	W	1	-	-	-	PSCAN	RGL_EN	0	Mode[1:0]	
	W	1	X[7:0]							
	W	1	-	-	-	-	-	-	Y[9:8]	
	W	1	Y[7:0]							
	W	1	W[7:0]							
	W	1							L[9:8]	
	W	1	L[7:0]							

PSCAN: Partial Scan control

0: Partial Scan disable.

1: Partial Scan enable (Gate Scan within Display Window only)

RGL_EN: REGAL function control

0: REGAL function disable.

1: REGAL function enable.

MODE: Mode selection, register or OTP.

REG_EN	MODE[1:0]	Description	Mode
0	00	OTP mode-0 LUT	KWG (K/W/Gray)
	01	OTP mode-1 LUT	KW (K/W)
	1x	OTP mode-2 LUT	KWR (K/W/Red)
1	00	Registers (R20h / R22h) KWG LUT and (R26h) FT LUT	KWG (K/W/Gray)
	01		KW (K/W)
	1x	Registers (R21h / R23h / R24h / R25h) Red LUT	KWR (K/W/Red)

X[7:0]: X-axis Start Point. X-axis start point for update display window.

Y[9:0]: Y-axis Start Point. Y-axis start point for update display window.

W[7:0]: X-axis Window Width. X-axis width for update display window.

L[9:0]: Y-axis Window Width. Y-axis width for update display window.

17-11) R13H (DTM2): Data Start Transmission 2

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	W	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**
	W	1	Pixel0[1:0]		Pixel1[1:0]		Pixel2[1:0]-		Pixel3[1:0]	
	W	1	…		…		…		…	
	W	1	Pixel(N-4)[1:0]		Pixel(N-3)[1:0]		Pixel(N-2)[1:0]		Pixel(N-1)[1:0]	

This command indicates that user starts to transmit data. Then write to new SRAM**:**

	Source Driver Output	
	DDX=1(Default)	DDX=0
Pixel[1:0]	LUT	LUT
00	Black	White
01	-	-
10	-	-
11	White	Black

17-12) R14H (DTMW): Data Start Transmission Window Register

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
(8 byte command)	W	0	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**
	W	1	X[7:0]							
	W	1	-	-	-	-	-	-	Y[9:8]	
	W	1	Y[7:0]							
	W	1	W[7:0]							
	W	1							L[9:8]	
	W	1	L[7:0]							

This command indicates the window before user start to transmit data.

The window is defined by (X, Y, W, L). X and W should be 4n format where n is integer.

17-13) R15H (DTM3): Data Start Transmission 3

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	W	0	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**
	W	1	Pixel 0	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7
	W	1	…	…	…	…	…	…	…	…
	W	1	Pixel(N-8)	Pixel(N-7)	Pixel(N-6)	Pixel(N-5)	Pixel(N-4)	Pixel(N-3)	Pixel(N-2)	Pixel(N-1)

This command transmitting old data to SRAM using KW mode only.

Pixel[0]: data bit for KW,

0: Black

1: White

Source Driver (KW Mode)		
	DDX=1 (Default)	DDX=0
Data	LUT	LUT
0	Black	White
1	White	Black

17-14) R16H (DTM4): Data Start Transmission 4

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	W	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**
	W	1	Pixel 0	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7
	W	1	…	…	…	…	…	…	…	…
	W	1	Pixel(N-8)	Pixel(N-7)	Pixel(N-6)	Pixel(N-5)	Pixel(N-4)	Pixel(N-3)	Pixel(N-2)	Pixel(N-1)

This command transmitting old data to SRAM using KW mode only.

Pixel[0]: data bit for KW,

0: Black

1: White

Source Driver (KW Mode)		
	DDX=1 (Default)	DDX=0
Data	LUT	LUT
0	Black	White
1	White	Black

17-15) R30H (LPRD): PLL Control

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	W	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**
	W	1	**LCLK[7:0]**							

The command controls the PLL clock frequency. The PLL structure supports the following frame rates:

(FR: Frame Rate, Unit: Hz)

LCLK[7:0]: Line Period Setting. Specify clock cycle number of 1MHz for one line period. (LCLK >=4)

04h: 5 clock cycles

12h: 19 clock cycles

17-16) R40H (TSC) Temperature Sensor Command

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	W	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
	R	1	D[10:3] or TS[7:0]							
	R	1	D[2:0]			**-**	**-**	**-**	**-**	**-**

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]	Temperature(℃)
1100 1110b	-25
1100 1111b	-24.5
1101 0000b	-24.5
:	:
1111 1110b	-1
1111 1111b	-0.5
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
:	:
0101 1010b	45
:	:
0110 0011b	49.5
0110 0100b	50

17-17) R41H (TSE) Temperature Sensor Enable

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	W	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**
	W	1	TSE	-	-	-	TO[3:0]			

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature Offset

TO[3:0]	Temperature Offset	TO[3:0]	Temperature Offset
0000	+0(Default)	1000	-8.0
0001	+1.0	1001	-7.0
0010	+2.0	1010	-6.0
0011	+3.0	1011	-5.0
0100	+4.0	1100	-4.0
0101	+5.0	1101	-3.0
0110	+6.0	1110	-2.0
0111	+7.0	1111	-1.0

17-18) R42H (TSW) Temperature Sensor Write

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	W	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**
	W	1	WATTR[7:0]							
	W	1	WMSB[7:0]							
	W	1	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6]: I^2C Write Byte Number

00 : 1 byte (head byte only)

01 : 2 bytes (head byte + pointer)

10 : 3 bytes (head byte + pointer + 1st parameter)

11 : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

17-19) R43H (TSR) Temperature Sensor Read

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	W	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
	W	1	RMSB[7:0]							
	W	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

17-20) R50H (CDI) VCOM and Data interval setting

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	W	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**
	W	1	BDZ	BDV	VBD[1:0]		-	-	-	DDX
	W	1	DCI[3:0]				-	-	CDI[9:8]	
	W	1	CDI[7:0]							

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept
(20 Hsync).

BDZ: Border Hi-Z control
- 0: Border Output Hi-Z disabled. (default)
- 1: Border Output Hi-Z enabled

BDV: Border DC Voltage control
- 0: Border Output DC Voltage Function disabled. (default)
- 1: Border Output DC Voltage Function enabled.

VBD[1:0]: Border output selection

DDX[1:0]: Data polarity.

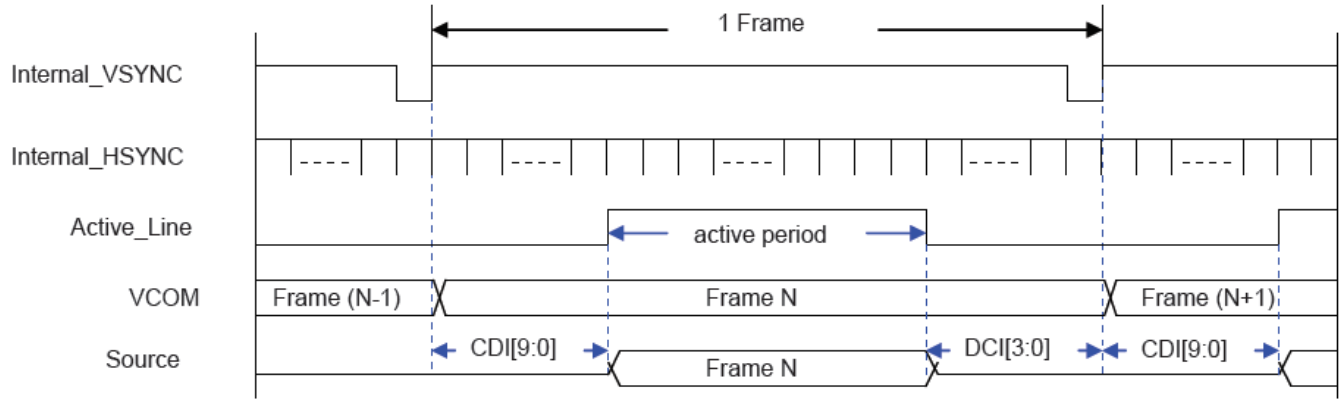
	Border Output	
	DDX=1(Default)	DDX=0
VBD[1:0]	LUT	LUT
00	Black	White
01	-	-
10	-	-
11	White	Black

DCI[3:0]: Source to VCOM interval. Interval time setting from source data to VCOM**.**

0000b ~ 1111b: 1 Hsync ~ 16 Hsync, respectively. **(Default: 001b: 4 Hsync)**

CDI[9:0]: VCOM to Source interval. Interval time setting from VCOM to source dat**.**

000 0000 000b ~ 11 1111 1111b: 1 Hsync ~ 1023 Hsync, respectively. **(Default: 018h: 25 Hsync)**



17-21) R51H (LPD) Low Power Detection

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	W	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**
	W	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (V_{DD}<2.2V/2.3V/2.4V/2.5V) 1: Normal status (default)

17-22) R61H (TRES) Resolution Setting

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	W	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
	W	1	0	1	1	1	1	1	1	1
	W	1	0	0	0	0	0	0	0	0
	W	1	1	1	1	1	1	1	1	1

17-23) R70H (REV) Revision

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	W	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**
	W	1	**LUTVER0[7:0]**							
	W	1	**LUTVER1[7:0]**							

LUTVER0[7:0]: LUT version 0 (Located in internal OTP address: F81h)

LUTVER1[7:0]: LUT version 1 (Located in internal OTP address: F82h)

This command only active when BUSY_N=”1”.

17-24) R71H (FLG) Get Status

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	W	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
	W	1	**-**	**-**	I^2C_ERR	I^2C_BUSYN	data_flag	PON	POF	BUSY_N

This command reads the IC status.

I^2C_ERR: I^2C master error status

I^2C_BUSYN: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

17-25) R81H (VV) VCOM value

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	R	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	R	1	-	VV[6:0]						

This command gets the Vcom value.

VV[6:0]: Vcom Value

VV[6:0]	VCOM Value
000 0000b	-0.1V
000 0001b	-0.15V
000 0010b	-0.20V
000 0011b	-0.25V
000 0100b	-0.30V
:	:
100 1110b	-4.0V
(others)	-4.0V

17-26) R82H (VDCS) VCM_DC Setting

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	W	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
	W	1	**-**	VDCS[60]						

This command sets VCOM_DC value

VDCS[6:0]: Vcom_DC setting

VDCS[6:0]	VCOM_DC value
000 0000b	-0.1V
000 0001b	-0.15V
000 0010b	-0.20V
000 0011b	-0.25V
000 0100b	-0.30V
:	:
100 1110b	-4.0V
(others)	-4.0V

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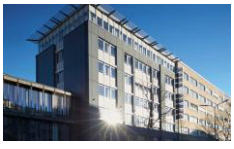

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