

# Specification

## **G104ACE-LH1**

10.4" - 800 x 600 – LVDS

Spec Revision: 2.0  
Revision Date: 24.10.2023

Note: This specification is subject to change without prior notice



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## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

G104ACE-LH1 is a 10.4" TFT Liquid Crystal Display IAV module with LED Backlight units and 30 pins LVDS interface. This module supports 800 x 600 SVGA mode and can display 16.7M/262k colors.

The PSWG is to establish a set of displays with standard mechanical dimensions and select electrical interface requirements for an industry standard 10.4" SVGA LCD panel and the LED driving device for Backlight is built in PCBA.

### 1.2 FEATURE

- Wide viewing angle
- High contrast ratio
- Fast response time
- SVGA ( 800 x 600 pixels) resolution
- DE (Data Enable) only mode
- LVDS Interface with 1pixel/clock
- PSWG (Panel Standardization Working Group)
- Wide operating temperature.
- RoHS compliance

### 1.3 APPLICATION

- TFT LCD Monitor
- Factory Application
- Amusement

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	211.2 (H) x 158.4(V) (10.4" diagonal)	mm	(1)
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	800 x R.G.B x 600	pixel	-
Pixel Pitch	0.264(H) x 0.264(W)	mm	-
Pixel Arrangement	RGB vertical Stripe	-	-
Display Colors	16.7M / 262K	color	-
Display Mode	Normally Black	-	-
Surface Treatment	Hard Coating (2H), Anti-Glare	-	-
Module Power Consumption	5.2	W	Typ.

**1.5 MECHANICAL SPECIFICATIONS**

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	242.5	243	243.5	mm	(1)
	Vertical(V)	183.5	184	184.5	mm	
	Depth(D)	7.5	8	8.5	mm	
Bezel Area	Horizontal	213.9	214.2	214.5	mm	-
	Vertical	161.3	161.6	161.9	mm	
Active Area	Horizontal	-	211.2	-	mm	
	Vertical	-	158.4	-	mm	
Weight		-	400	420	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

**2. ABSOLUTE MAXIMUM RATINGS**

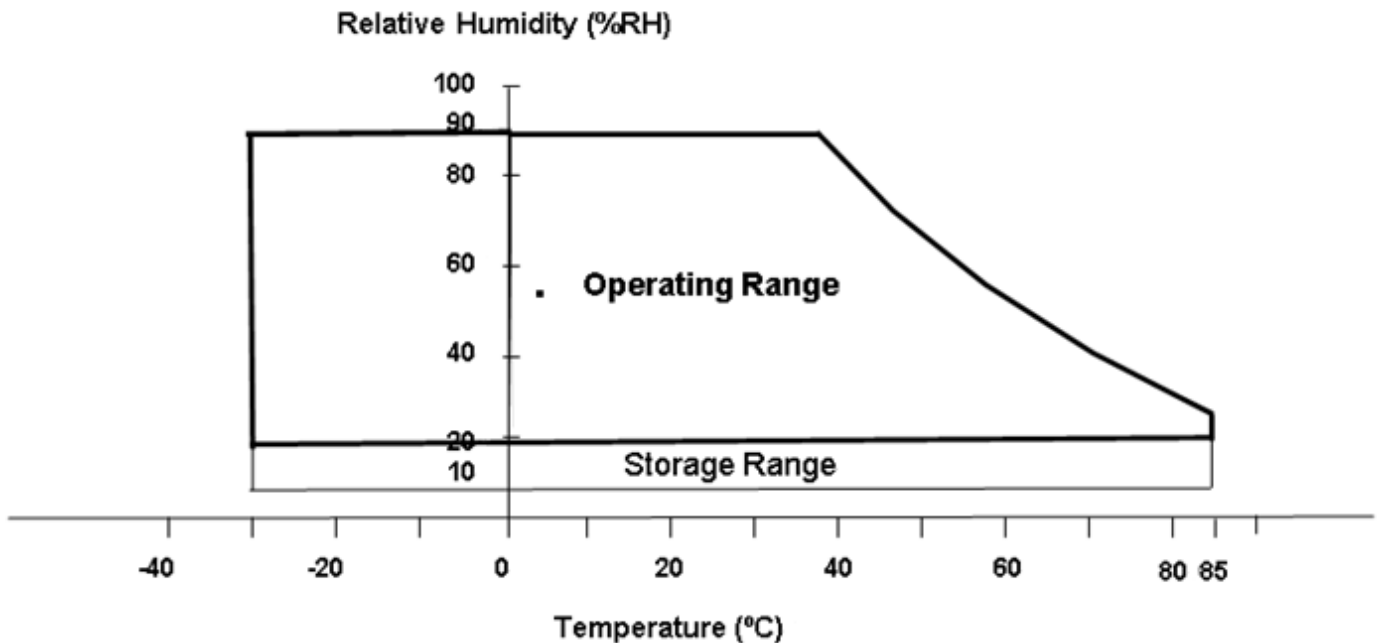
**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Operating Ambient Temperature	T <sub>OP</sub>	-30	+85	°C	(1)(2)
Storage Temperature	T <sub>ST</sub>	-30	+85	°C	

Note (1)

- (a) 90 %RH Max.
- (b) Wet-bulb temperature should be 39 °C Max.
- (c) No condensation.

Note (2) Panel surface temperature should be 0°C min. and 85°C max under Vcc=5.0V, fr =60Hz, typical LED string current, 25°C ambient temperature, and no humidity control . Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 85°C (Panel surface temperature).





## 2.2 ELECTRICAL ABSOLUTE RATINGS

### 2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	5.5	V	(1)
Logic Input Voltage	V <sub>IN</sub>	-0.3	3.6	V	

### 2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Converter Voltage	V <sub>i</sub>	-0.3	18	V	(1), (2)
Enable Voltage	EN	---	5.5	V	
Backlight Adjust	Dimming	---	5.5	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to 3.2 for further information).

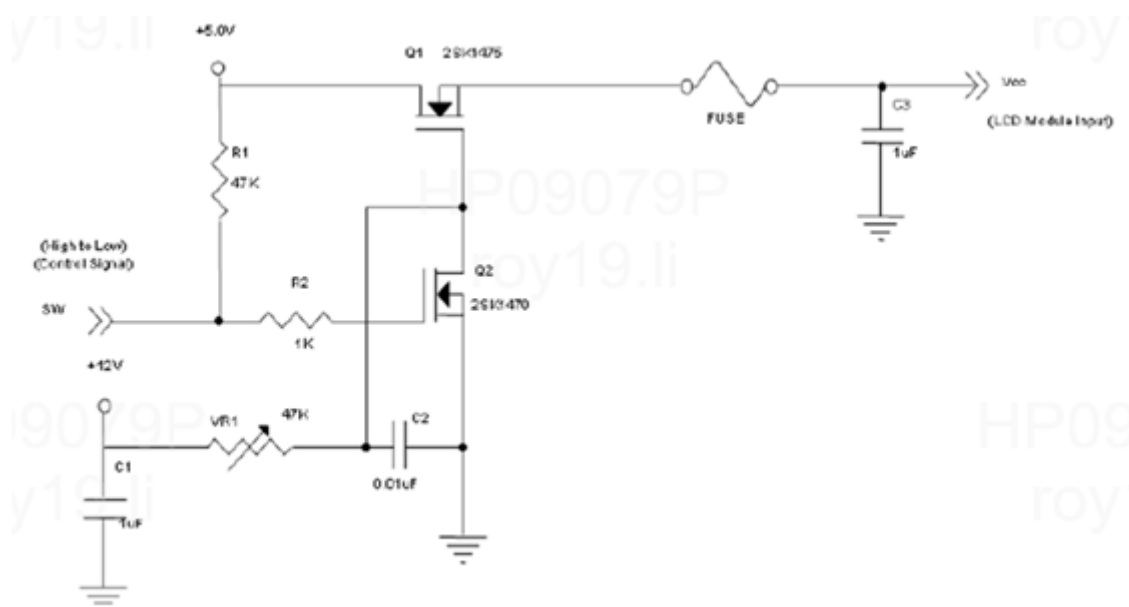
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

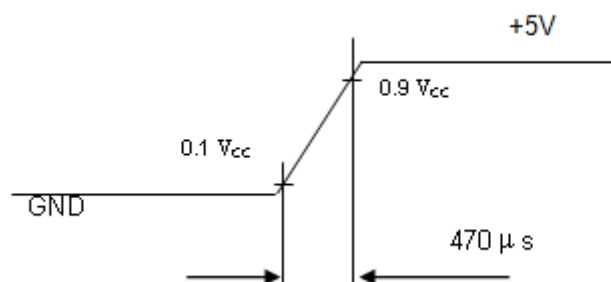
Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Power Supply Voltage	$V_{CC}$	4.5	5	5.5	V	-	
Ripple Voltage	$V_{RP}$	-	-	300	mVp-p		
Inrush Current	$I_{INRUSH}$	-	-	2.5	A	(2)	
Power Supply Current	White	-	195	235	mA	(3)a	
	Black	-	85	105	mA	(3)b	
LVDS differential input voltage	$V_{id}$	200	-	600	mV	(5)	
LVDS common input voltage	$V_{ic}$	1.0	1.2	1.4	V	(5)	
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	$V_{IH}$	-	-	100	mV	-
	"L" Level	$V_{IL}$	-100	-	-	mV	-
Terminating Resistor	$R_T$	-	100	-	Ohm	-	

Note (1)The module should be always operated within above ranges.

Note (2)Measurement Conditions:

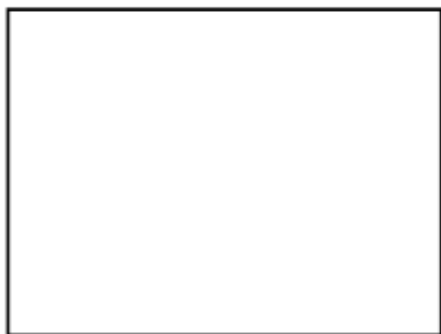


VCC rising time is 470μ s



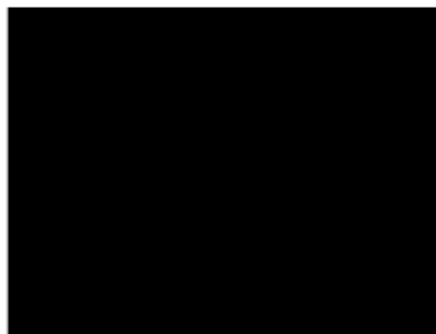
Note (3) The specified power supply current is under the conditions at  $V_{DD} = 5V$ ,  $T_a = 25 \pm 2 \text{ }^\circ\text{C}$ , DC Current and  $f_v = 60 \text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

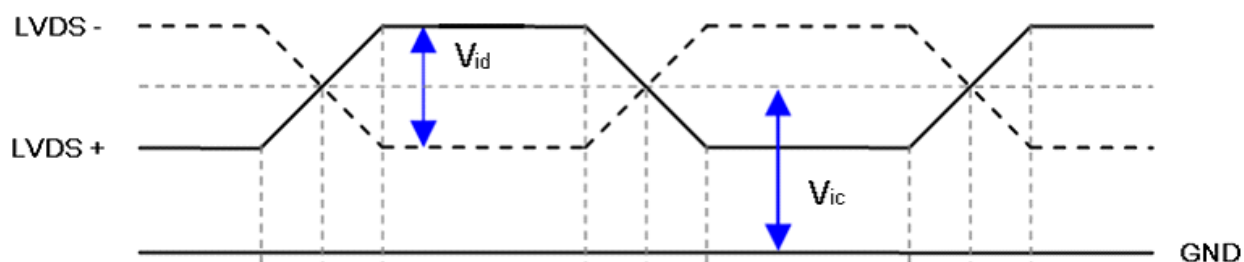
b. Black Pattern



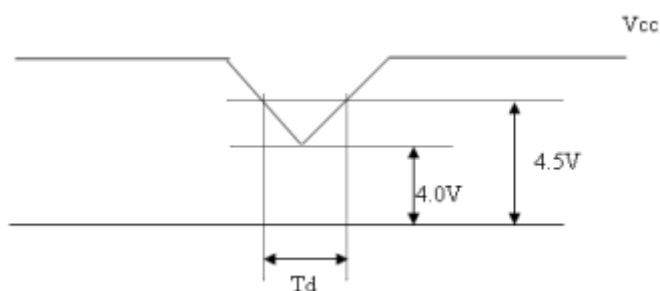
Active Area

Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition



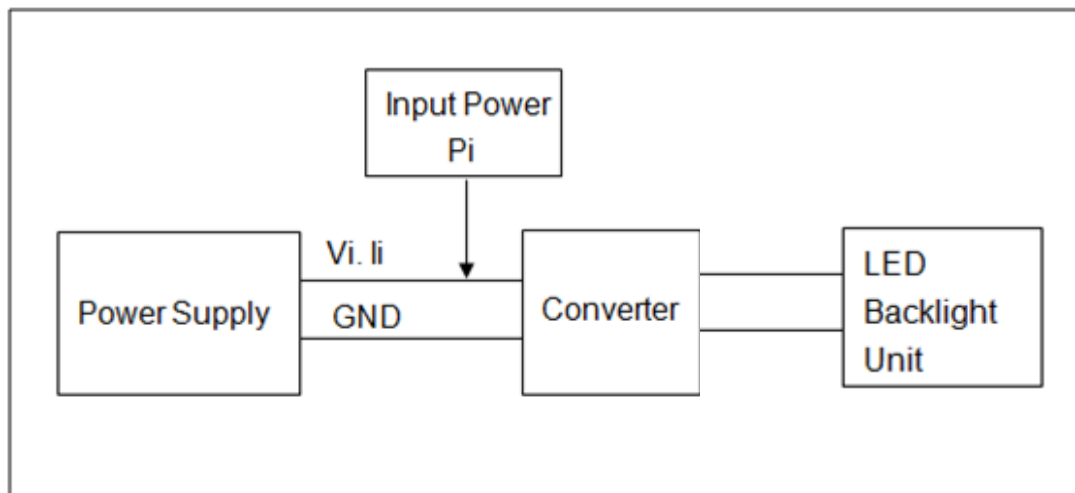
Note (6) Dip condition:  $4.0V \leq V_{cc} \leq 4.5V$ ,  $T_d \leq 20ms$



3.2 BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Converter Input Voltage	$V_i$	10.8	12.0	13.2	$V_{DC}$	(Duty 100%)	
Converter Input Ripple Voltage	$V_{IRP}$	-	-	350	mV		
Converter Input Current	$I_i$	-	0.35	0.41	$A_{DC}$	@ $V_i = 12V$ (Duty 100%)	
Converter Inrush Current	$I_{IRUSH}$	-	-	3.0	A	@ $V_i$ rising time=20ms ( $V_i=12V$ )	
Input Power Consumption	$P_i$	-	4.2		W	(1), @ $V_i = 12V$ (Duty 100%)	
EN Control Level	Backlight on	ENLED (BLON)	2.5	3.3	5.0	V	
	Backlight off		0	-	0.3	V	
PWM Control Level	PWM High Level	Dimming (E_PWM)	2.5	-	5.0	V	
	PWM Low Level		0	-	0.15	V	
PWN Noise Range	$V_{Noise}$		-	-	0.1	V	
PWM Control Frequency	$f_{PWM}$		190	200	20k	Hz	(2)
PWM Dimming Control Duty Ratio			5	-	100	%	(2), @ $190Hz < f_{PWM} < 1kHz$
			20	-	100	%	(2), @ $1kHz \leq f_{PWM} < 20kHz$
LED Life Time	$L_{LED}$		50,000		-	Hrs	(3)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) At 190 ~1kHz PWM control frequency, duty ratio range is restricted from 5% to 100%.

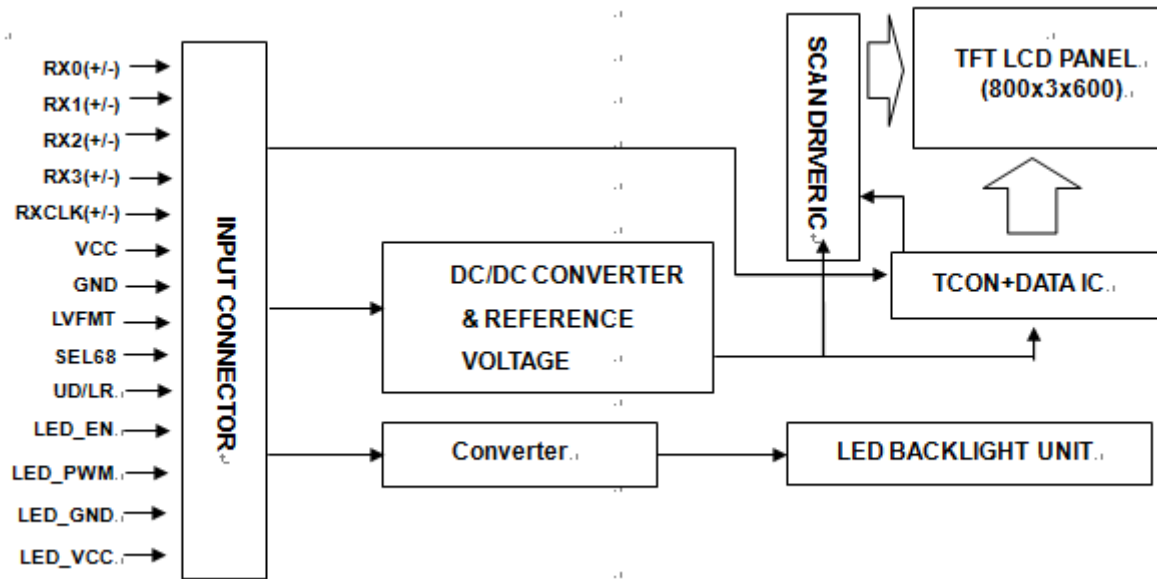
1K ~20kHz PWM control frequency, duty ratio range is restricted from 20% to 100%.

If PWM control frequency is applied in the range from 1KHz to 20KHZ, The“non-linear”phenomenon on the Backlight Unit may be found. So It’s a suggestion that PWM control frequency should be less than 1KHz.

Note (3) The lifetime of LED is estimated data and defined as the time when it continues to operate under the conditions at  $T_a = 25 \pm 2 \text{ }^\circ\text{C}$  and Duty 100% until the brightness becomes  $\leq 50\%$  of its original value. Operating LED at high temperature condition will reduce life time and lead to color shift.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



## 5. INPUT TERMINAL PIN ASSIGNMENT

### 5.1 TFT LCD MODULE

Pin No.	Symbol	Function	Polarity	Note
1	RX00-	Negative LVDS differential data input. Channel O0	Negative	
2	RX00+	Positive LVDS differential data input. Channel O0	Positive	
3	RX01-	Negative LVDS differential data input. Channel O1	Negative	
4	RX01+	Positive LVDS differential data input. Channel O1	Positive	
5	RX02-	Negative LVDS differential data input. Channel O2	Negative	
6	RX02+	Positive LVDS differential data input. Channel O2	Positive	
7	GND	Ground		
8	RXOC-	Negative LVDS differential clock input.	Negative	
9	RXOC+	Positive LVDS differential clock input.	Positive	
10	RX03-	Negative LVDS differential data input. Channel O3	Negative	
11	RX03+	Positive LVDS differential data input. Channel O3	Positive	
12	GND	Ground		
13	LVFMT	LVDS VESA / JEIDA select function control, NC → VESA Format (Default).; Low → JEIDA Format		(3)(4)
14	LED_PWM	Backlight Adjust (PWM Dimming 190-210Hz,H: 3.3VDC, L: 0VDC)		
15	LED_EN	Enable pin 3.3V		
16	LED_GND	Converter ground		
17	LED_GND	Converter ground		
18	LED_GND	Converter ground		
19	NC	Not connection, this pin should be open		
20	LED_VCC	Converter input voltage 12V		
21	LED_VCC	Converter input voltage 12V		
22	LED_VCC	Converter input voltage 12V		
23	NC	Not connection, this pin should be open		
24	NC	Not connection, this pin should be open		
25	SEL68	LVDS 6/8 bit select function control, Low → 6 bit Input Mode. High → 8bit Input Mode		(3)(4)
26	NC	Not connection, this pin should be open		
27	NC	Not connection, this pin should be open		
28	UD/LR	Reverse Scan Control, Low → Normal Mode. High → Reverse Scan		(3)(4)
29	VCC	Power supply 5V		
30	VCC	Power supply 5V		

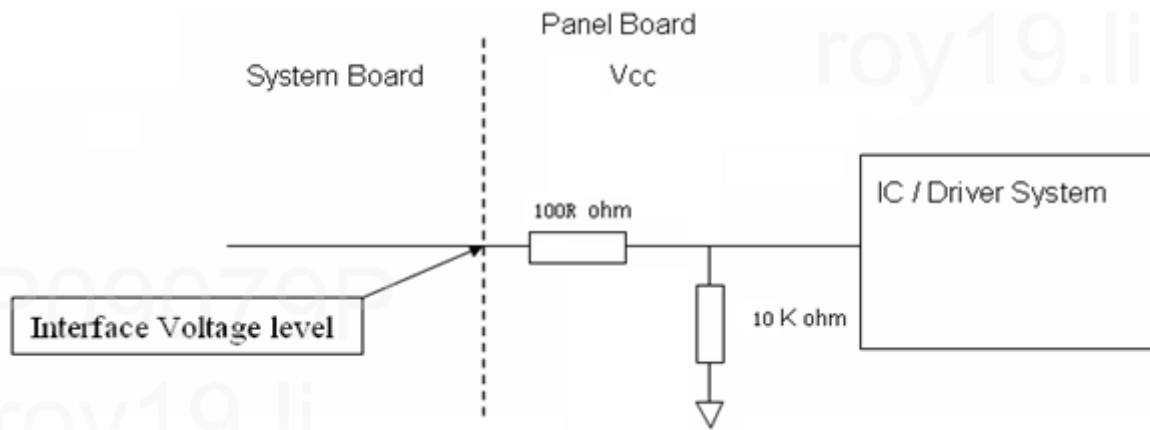
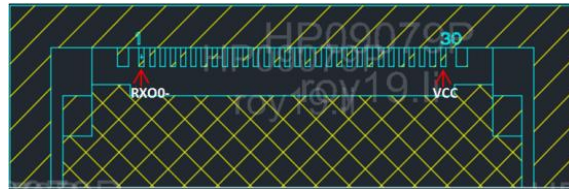
Note (1) Connector Part No.: STM MSAK24025P30MB(Exterior silver) or I-PEX 20455-030E-76(Exterior gold) or equivalent.

Note (2) User's connector Part No.: I-PEX20453-030T-03 or equivalent.

Note (3) "Low" stands for 0V. "High" stands for 3.3V.

Note (4) Interface optional pin has internal scheme as following diagram, Customer should keep the interface voltage level requirement which including panel board loading as below.

Note (5) Pin1 location is RX00- to comply with mechanical characteristics



## 5.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0		
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1		

Note (1)0: Low Level Voltage, 1: High Level Voltage



The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green(1)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
Green(2)		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
Green(253)		0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0		
Green(254)		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
Green(255)		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0		
Gray Scale Of Blue		Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	

Note (1)0: Low Level Voltage, 1: High Level Voltage

**6. INTERFACE TIMING**

**6.1 INPUT SIGNAL TIMING SPECIFICATIONS**

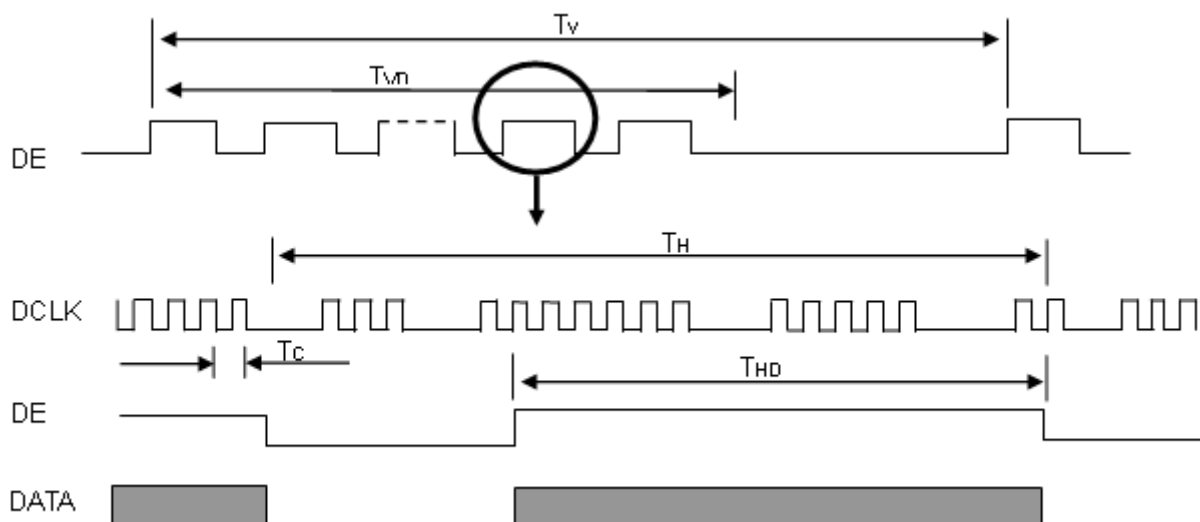
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	$F_r$	34	40	48	MHz	-
	Period	$T_c$	29.4	25	20.83	ns	
	Input Clock to data skew	TLVCCS	-	-	0.25	UI	(a)
	Spread spectrum modulation range	$F_{clkin\_mod}$	-1.5		1.5	%	(b)
	Spread spectrum modulation frequency	$F_{SSM}$	25	-	90	KHz	
Vertical Display Term	Frame Rate	$F_r$	60	60	60	Hz	-
	Total	$T_v$	610	628	760	$T_h$	$T_v=T_{vd}+T_{vb}$
	Active Display	$T_{vd}$	600	600	600	$T_h$	-
	Blank	$T_{vb}$	10	28	160	$T_h$	-
Horizontal Display Term	Total	$T_h$	970	1056	1100	$T_c$	$T_h=T_{hd}+T_{hb}$
	Active Display	$T_{hd}$	800	800	800	$T_c$	-
	Blank	$T_{hb}$	170	256	300	$T_c$	-

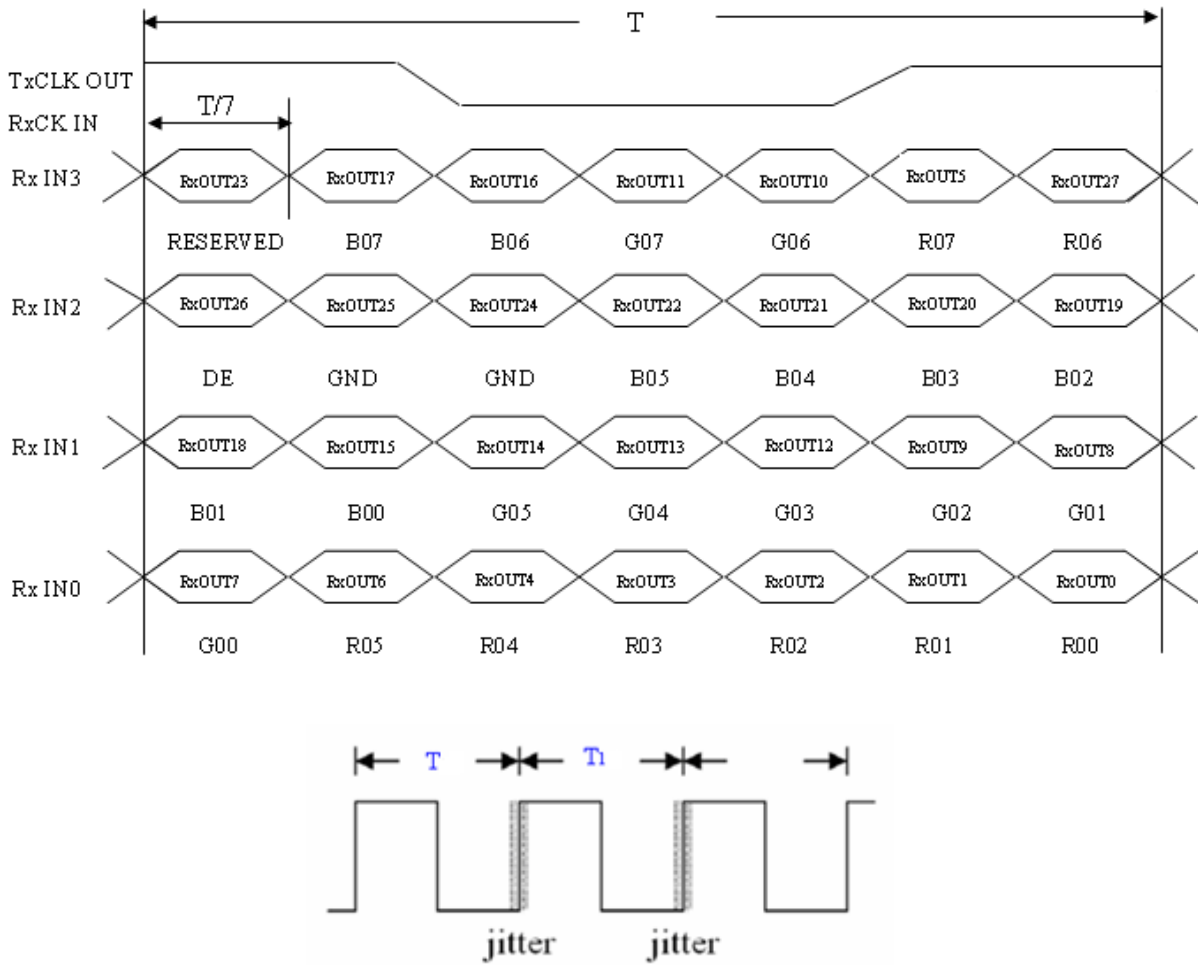
Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note (2) The  $T_v(T_{vd}+T_{vb})$  must be integer, otherwise, the module would operate abnormally.

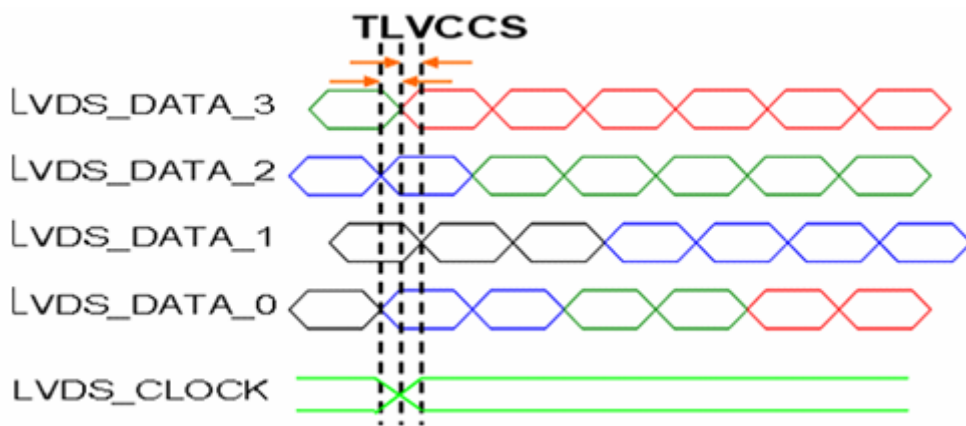
**INPUT SIGNAL TIMING DIAGRAM**



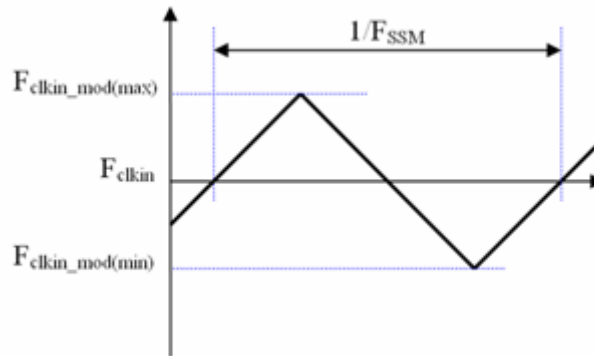
**TIMING DIAGRAM of LVDS**



Note (a) Input Clock to data skew is defined as below figures.

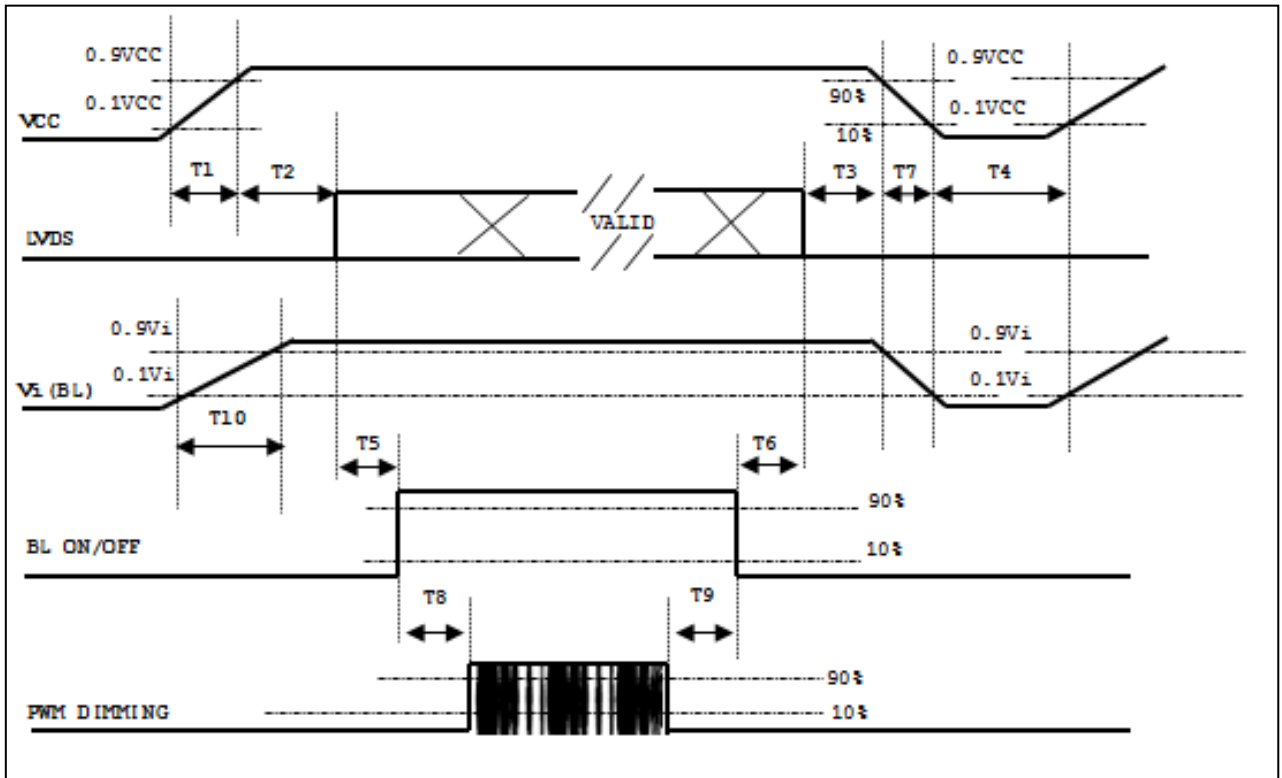


Note (b) The SSCG (Spread spectrum clock generator) is defined as below figures.



### 6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



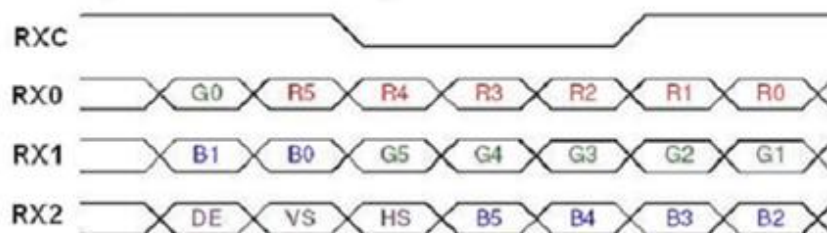
Parameter	Value			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	450	-	-	ms
T6	200	-	-	ms
T7	10	-	100	ms
T8	10	-	-	ms
T9	10	-	-	ms
T10	20	-	50	ms

**Note:**

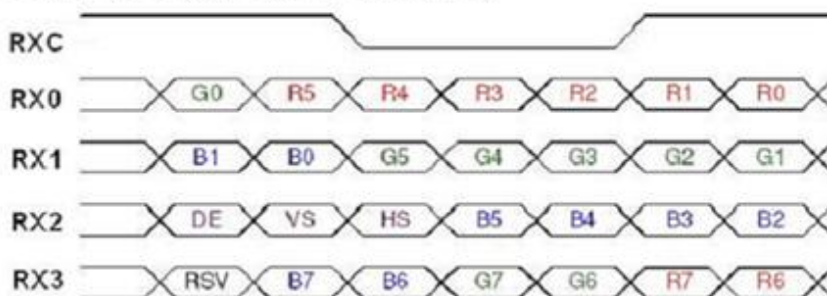
- (1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.
- (2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.
- (6) INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.
- (7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec".

6.3 The INPUT DATA FORMAT

**SEL 6/8="Low" for 6 Bits LVDS**



**SEL 6/8="High" for 8 Bits LVDS**



Note (1) R/G/B data 7: MSB, R/G/B data 0: LSB

Note (2) Please follow PSWG

Signal Name	Description	Remark
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.
G7 G6 G5 G4 G3 G2 G1 G0	Green Data 7 (MSB) GreenData 6 GreenData 5 GreenData 4 GreenData 3 GreenData 2 GreenData 1 GreenData 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2 B1 B0	Blue Data 7 (MSB) Blue Data 6 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.
RXCLKIN+ RXCLKIN-	LVDS Clock Input	
DE	Display Enable	
VS	Vertical Sync	
HS	Horizontal Sync	

**6.4 SCANNING DIRECTION**

The following figures show the image see from the front view. The arrow indicates the direction of scan.

**Fig.1 Normal Scan**



PCBA on the Top side

**Fig.2 Reverse Scan**



PCBA on the Top side

Fig. 1 Normal scan (pin 28, UD/LR = Low )

Fig. 2 Reverse scan (pin 28, UD/LR = Hight )

## 6.5. LVDS INPUT SIGNAL SPECIFICATIONS

### 6.5.1 LVDS DATA INPUT DATA FORMAT (VESA/ JEIDA) - 6bit

LVDS Channel 0	LVDS output	<b>D7</b>	<b>D6</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>
	Data order	G0	R5	R4	R3	R2	R1	R0
LVDS Channel 1	LVDS output	<b>D18</b>	<b>D15</b>	<b>D14</b>	<b>D13</b>	<b>D12</b>	<b>D9</b>	<b>D8</b>
	Data order	B1	B0	G5	G4	G3	G2	G1
LVDS Channel 2	LVDS output	<b>D26</b>	<b>D25</b>	<b>D24</b>	<b>D22</b>	<b>D21</b>	<b>D20</b>	<b>D19</b>
	Data order	DE	GND	GND	B5	B4	B3	B2

Note (1) Pin 13, LVFMT =NC

### 6.5.2 LVDS DATA INPUT DATA FORMAT (VESA) - 8bit

LVDS Channel 0	LVDS output	<b>D7</b>	<b>D6</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>
	Data order	G0	R5	R4	R3	R2	R1	R0
LVDS Channel 1	LVDS output	<b>D18</b>	<b>D15</b>	<b>D14</b>	<b>D13</b>	<b>D12</b>	<b>D9</b>	<b>D8</b>
	Data order	B1	B0	G5	G4	G3	G2	G1
LVDS Channel 2	LVDS output	<b>D26</b>	<b>D25</b>	<b>D24</b>	<b>D22</b>	<b>D21</b>	<b>D20</b>	<b>D19</b>
	Data order	DE	GND	GND	B5	B4	B3	B2
LVDS Channel 3	LVDS output	<b>D23</b>	<b>D17</b>	<b>D16</b>	<b>D11</b>	<b>D10</b>	<b>D5</b>	<b>D27</b>
	Data order	NA	B7	B6	G7	G6	R7	R6

Note (2) Pin 13, LVFMT =NC

### 6.5.3 LVDS DATA INPUT DATA FORMAT (JEIDA) - 8bit

LVDS Channel 0	LVDS output	<b>D7</b>	<b>D6</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>
	Data order	G2	R7	R6	R5	R4	R3	R2
LVDS Channel 1	LVDS output	<b>D18</b>	<b>D15</b>	<b>D14</b>	<b>D13</b>	<b>D12</b>	<b>D9</b>	<b>D8</b>
	Data order	B3	B2	G7	G6	G5	G4	G3
LVDS Channel 2	LVDS output	<b>D26</b>	<b>D25</b>	<b>D24</b>	<b>D22</b>	<b>D21</b>	<b>D20</b>	<b>D19</b>
	Data order	DE	GND	GND	B7	B6	B5	B4
LVDS Channel 3	LVDS output	<b>D23</b>	<b>D17</b>	<b>D16</b>	<b>D11</b>	<b>D10</b>	<b>D5</b>	<b>D27</b>
	Data order	NA	B1	B0	G1	G0	R1	R0

Note (3) Pin 13, LVFMT =GND

Note(4): Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally



## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value and tolerance in "ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown here and all items are measured at the center point of screen unless otherwise noted. The following items should be measured under the test conditions described above and stable conditions shown in Note (5).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	0.595	0.645	0.695	-	(1), (5)
		Ry	0.290	0.340	0.390		
	Green	Gx	0.270	0.320	0.370		
		Gy	0.555	0.605	0.655		
	Blue	Bx	0.102	0.152	0.202		
		By	0.000	0.050	0.100		
	White	Wx	0.263	0.313	0.363		
		Wy	0.279	0.329	0.379		
Center Luminance of White	LC		320	400			(4), (5)
Contrast Ratio	CR		800	1000			(2), (5)
Response Time	TR	$\theta X=0^\circ, \theta Y=0^\circ$	-	13	18	-	(3)
	TF		-	12	17	-	
White Variation	$\delta W$	$\theta X=0^\circ, \theta Y=0^\circ$	72	80	-	%	(5), (6)
Viewing Angle	Horizontal	$\theta X+$	80	89	-	Deg.	(1), (5)
		$\theta X-$	80	89	-		
	Vertical	$\theta Y+$	80	89	-		
		$\theta Y-$	80	89	-		

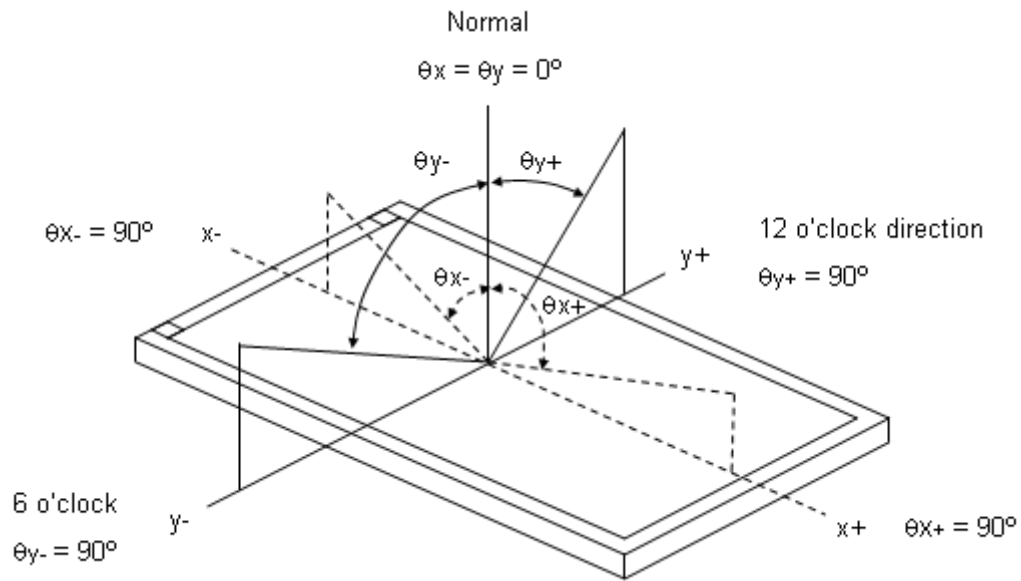
Definition :

Grayscale Maximum : Grayscale 255 (10 bits: grayscale 1023 ; 8 bits : grayscale 255 ; 6 bits: grayscale 63)

White : Luminance of Grayscale Maximum (All R,G,B)

Black : Luminance of grayscale 0 (All R,G,B)

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):

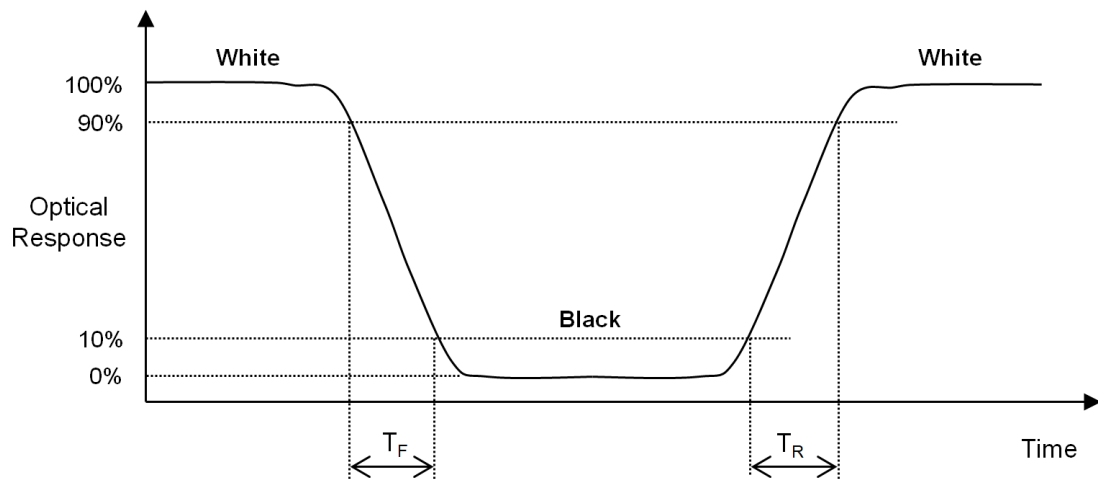


Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression at center point.

$$\text{Contrast Ratio (CR)} = \text{White} / \text{Black}$$

Note (3) Definition of Response Time ( $T_R, T_F$ ):

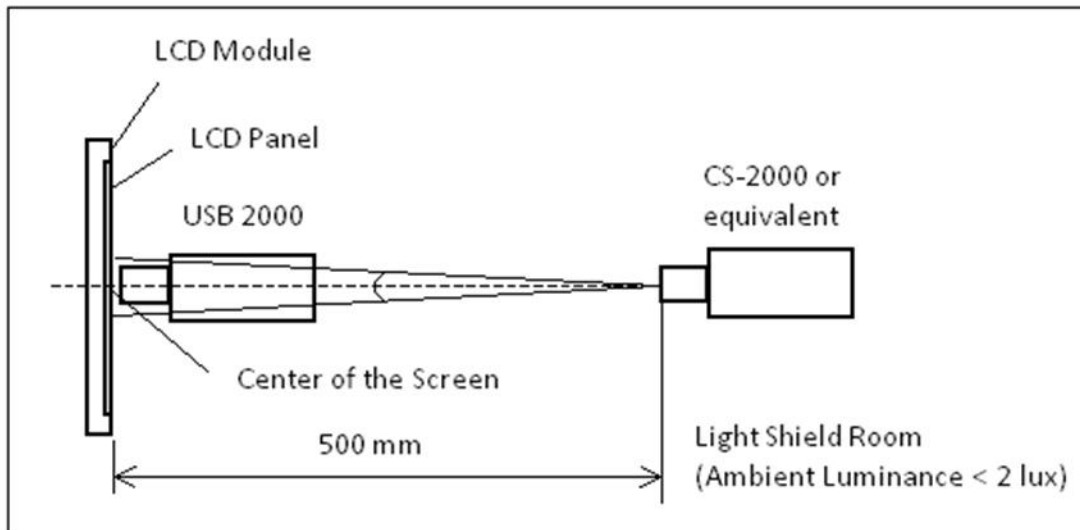


Note (4) Definition of Luminance of White ( $L_c$ ):

Measure the luminance of White at center point.

Note (5) Measurement Setup:

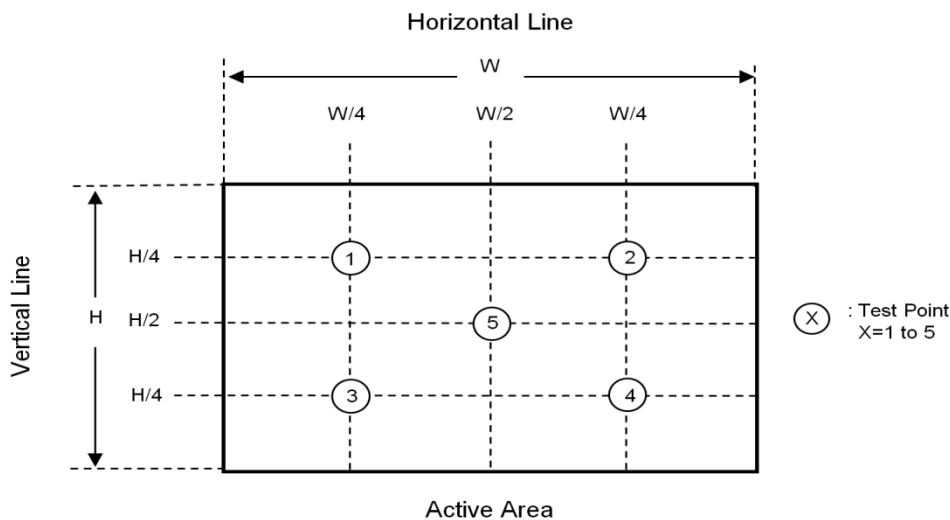
The LCD module should be stabilized at given temperature to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room. The measurement placement of module should be in accordance with module drawing.



Note (6) Definition of White Variation ( $\delta W$ ):

Measure the luminance of White at 5 points.

Luminance of White :  $L(X)$  , where X is from 1 to 5.



## 8. RELIABILITY TEST CRITERIA

Test Item	Test Condition	Note
High Temperature Storage Test	85°C, 240 hours	(1),(2) (4),(5)
Low Temperature Storage Test	-30°C, 240 hours	
Thermal Shock Storage Test	-30°C, 0.5 hour ↔ 70°C, 0.5 hour; 100cycles, 1 hour/cycle)	
High Temperature Operation Test	85°C, 240 hours	
Low Temperature Operation Test	-30°C, 240 hours	
High Temperature & High Humidity Operation Test	60°C, RH 90%, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1 sec/cycle Condition 1 : panel contact, ±8 KV Condition 2 : panel non-contact ±15 KV	(1), (4)
Shock (Non-Operating)	50G, 11ms, half sine wave, 1 time for ± X, ± Y, ± Z direction	(2), (3)
Vibration (Non-Operating)	1.5G, 10 ~ 300 Hz sine wave, 10 min/cycle, 3 cycles each X, Y, Z direction	

Note (1) There should be no condensation on the surface of panel during test ,

Note (2) Temperature of panel display surface area should be 85°C Max.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (4) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

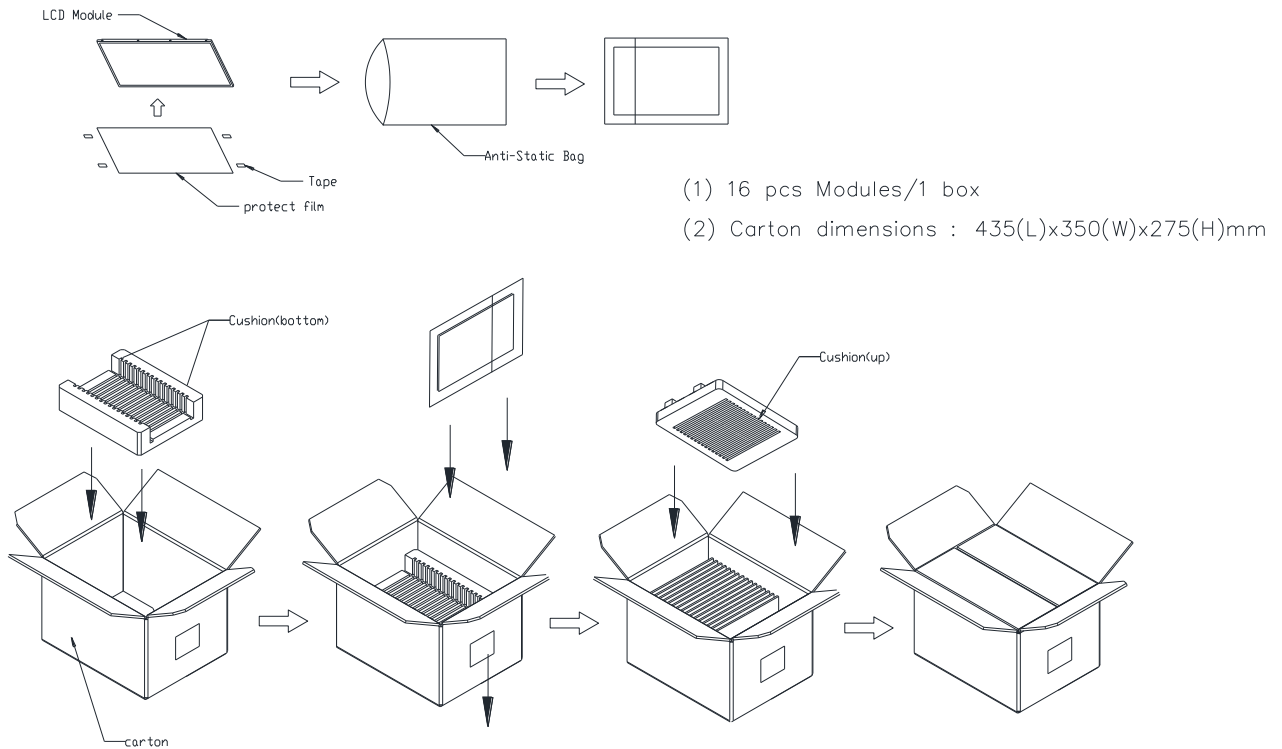
Note (5) Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

**9. PACKAGE**

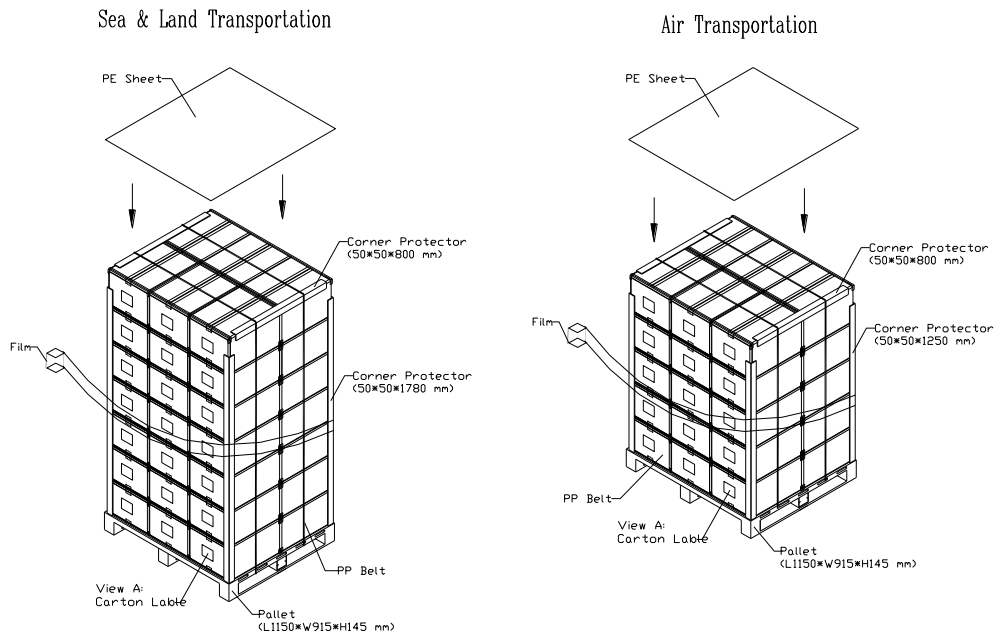
**9.1 PACKAGE SPECIFICATIONS**

- (1) 16pcs LCD modules / 1 Box
- (2) Box dimensions: 435 (L) X 350 (W) X 275 (H) mm
- (3) Weight: approximately 9.2Kg (16 modules per box)

**9.2 PACKAGE METHOD**

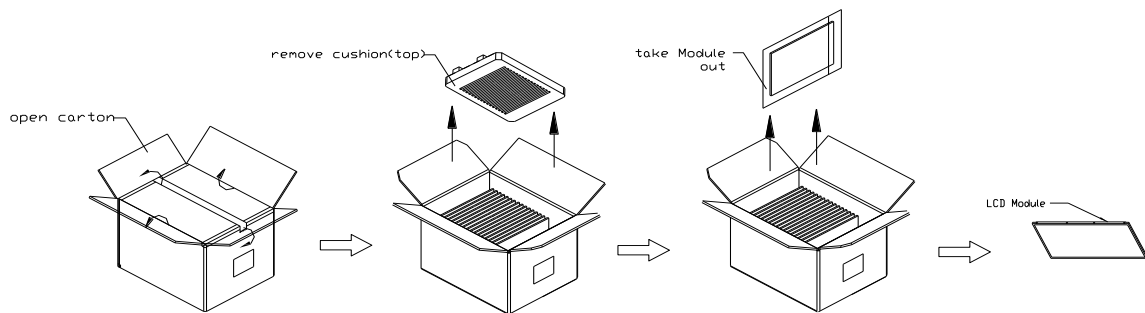


**Figure. 9-1 Packing method**



**Figure. 9-2 Packing method**

**9.3 UN- PACKAGE METHOD**

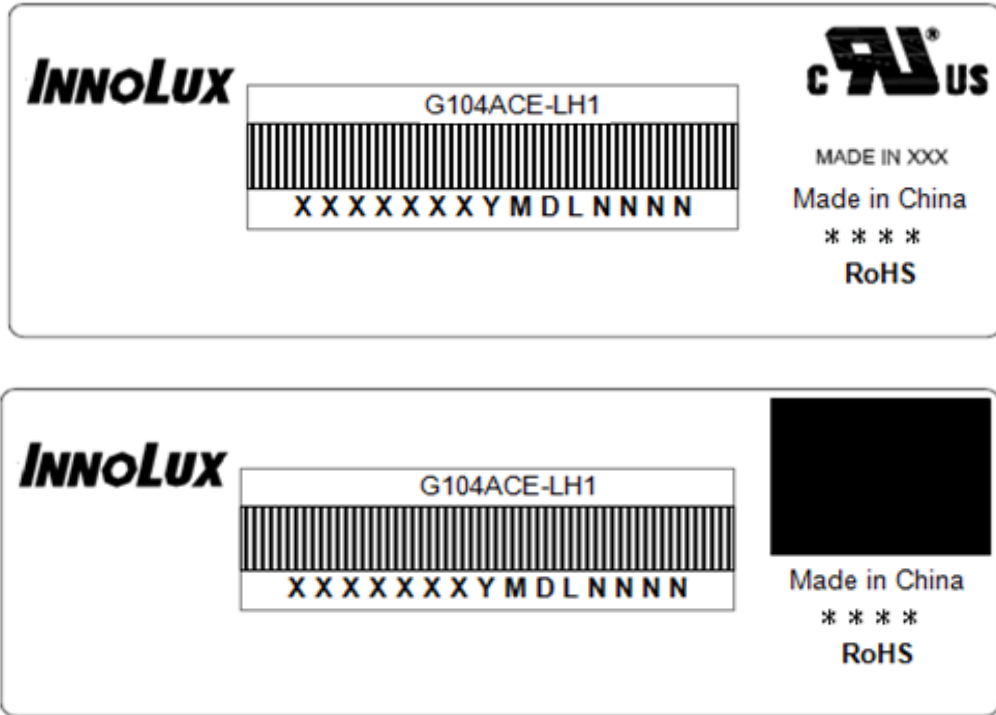


**Figure. 9-3 UN-Packing method**

**10. DEFINITION OF LABELS**

**10.1 INX MODULE LABEL**

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

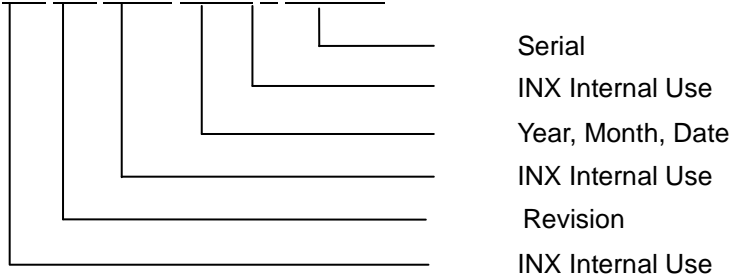


Note (1) Safety Compliance(UL logo) will open after C1 version.

(a) Model Name: G104ACE-LH1

(b) \* \* \* \* : Factory ID

(c) Serial ID: X X X X X X Y M D X N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2021~2029  
 Month: 1~9, A~C, for Jan. ~ Dec.  
 Day: 1~9, A~Y, for 1<sup>st</sup> to 31<sup>st</sup>, exclude I , O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

**11. PRECAUTIONS****11.1 ASSEMBLY AND HANDLING PRECAUTIONS**

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

**11.2 STORAGE PRECAUTIONS**

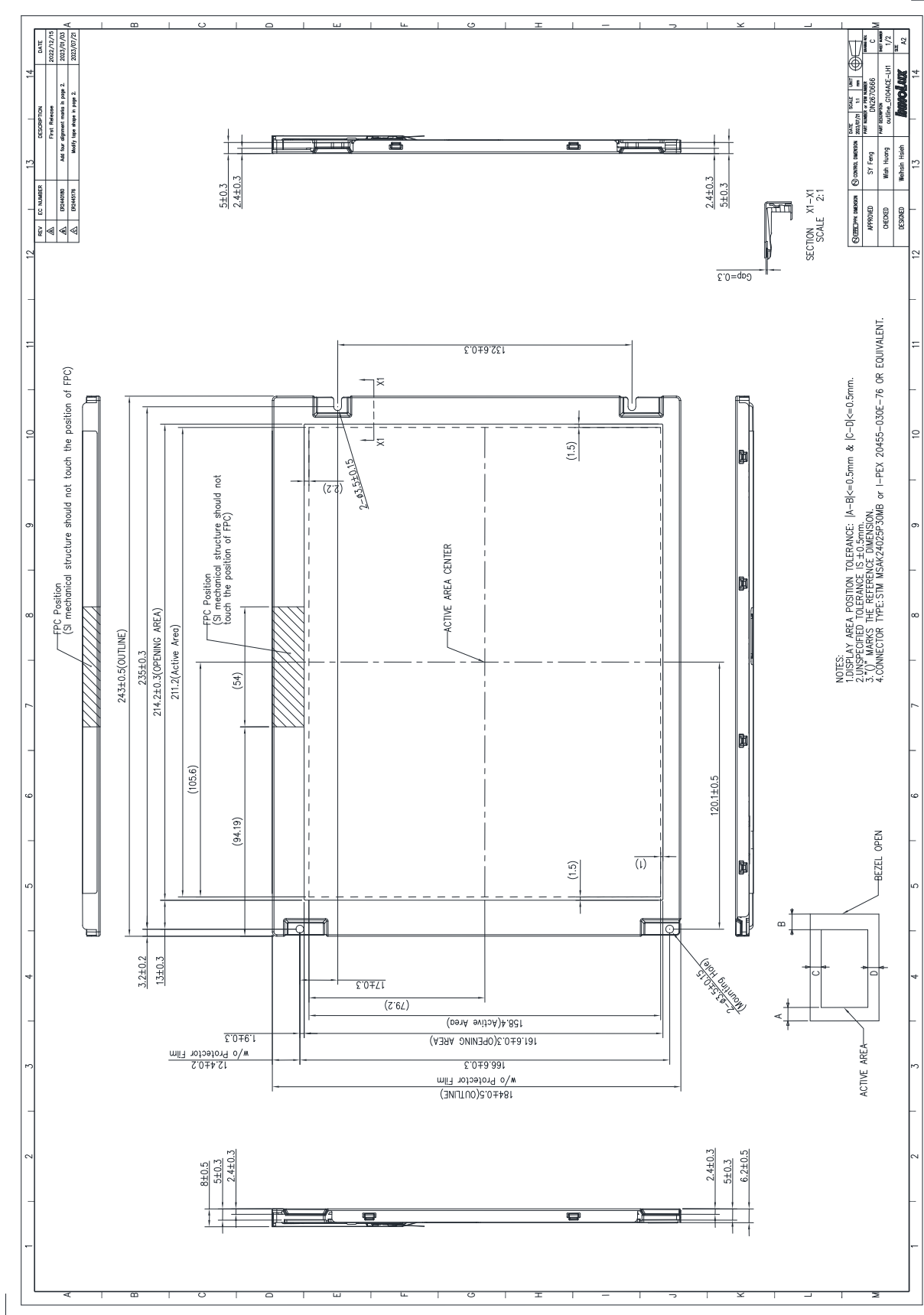
- (1) When storing for a long time, the following precautions are necessary.
  - (a) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 30°C at humidity 50+-10%RH.
  - (b) The polarizer surface should not come in contact with any other object.
  - (c) It is recommended that they be stored in the container in which they were shipped.
  - (d) Storage condition is guaranteed under packing conditions.
  - (e) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition
- (2) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (3) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (4) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

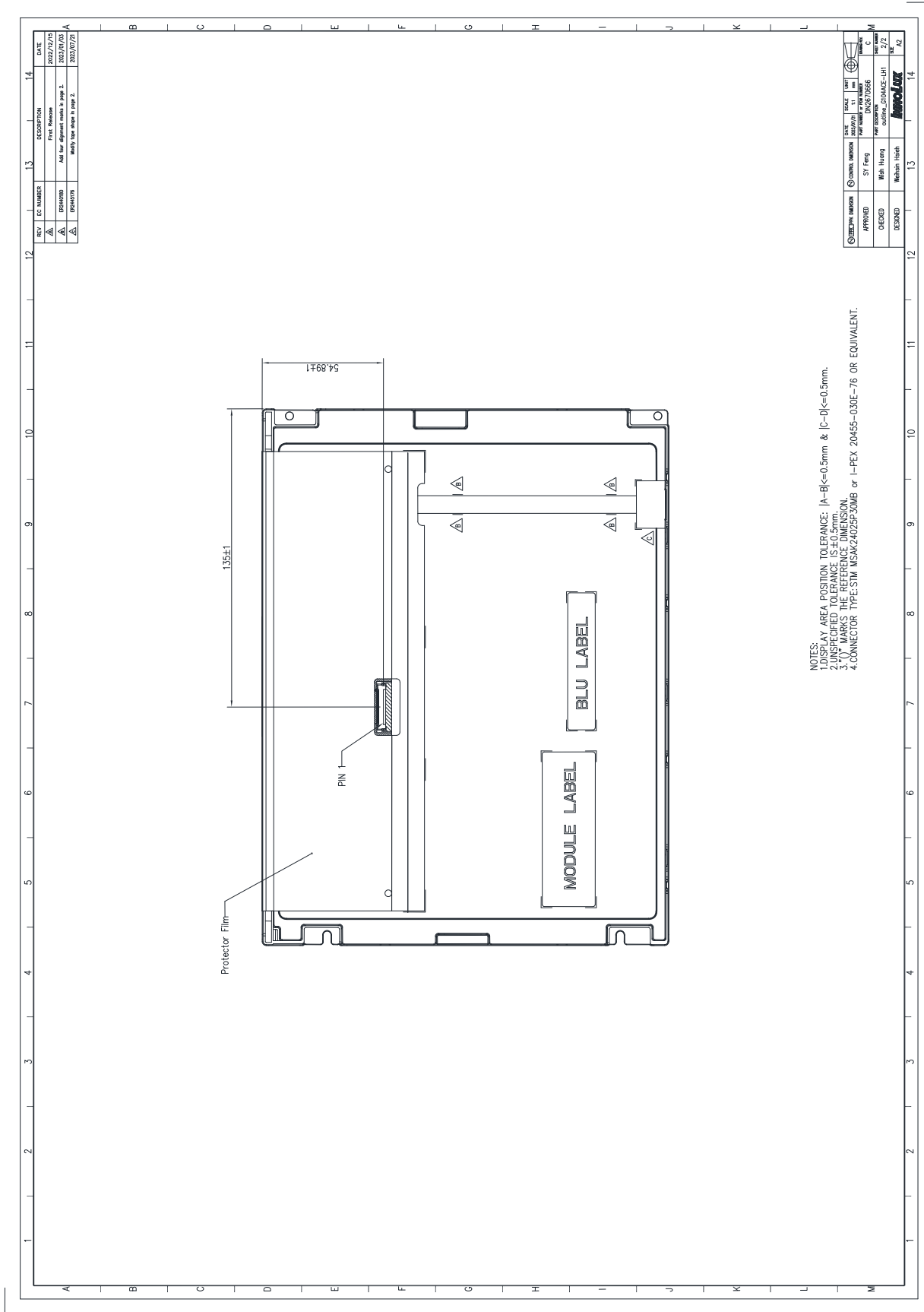


### 11.3 OTHER PRECAUTIONS

- (1) Normal operating condition
  - (a) Display pattern: dynamic pattern (Real display)
    - (Note) Long-term static display can cause image sticking.
- (2) Operating usages to protect against image sticking due to long-term static display
  - (a) Suitable operating time: under 16 hours a day.
  - (b) Static information display recommended to use with moving image.
  - (c) Cycling display between 5 minutes' information(static) display and 10 seconds' moving image
- (3) Abnormal condition just means conditions except normal condition.


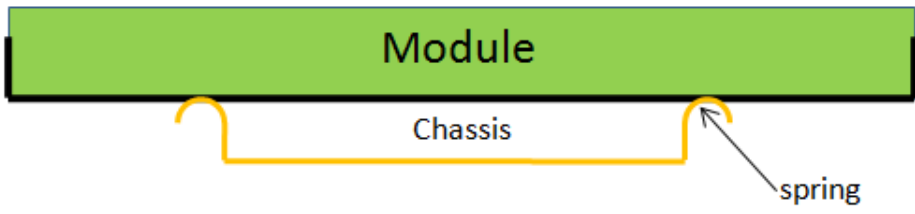

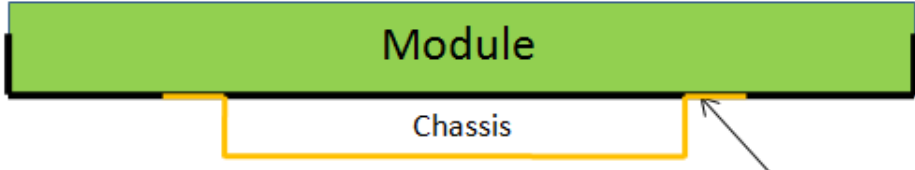
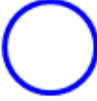
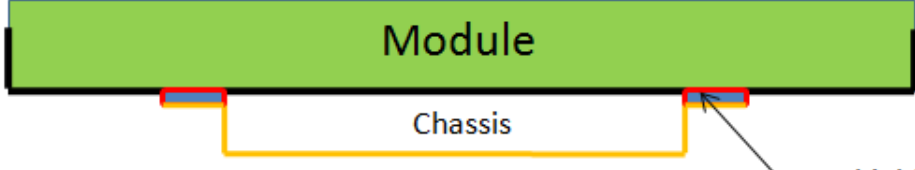
**12. MECHANICAL CHARACTERISTICS**



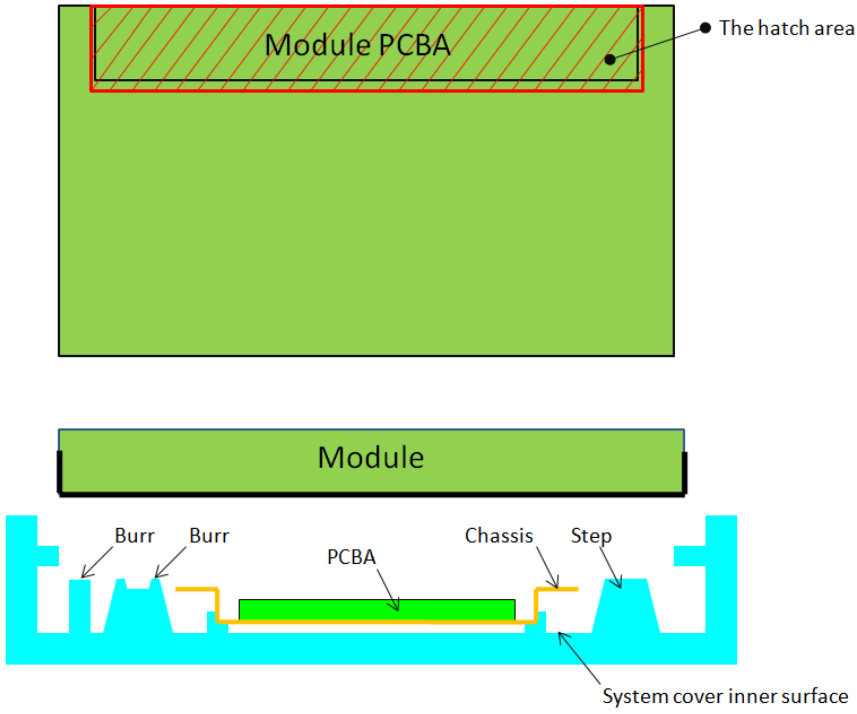


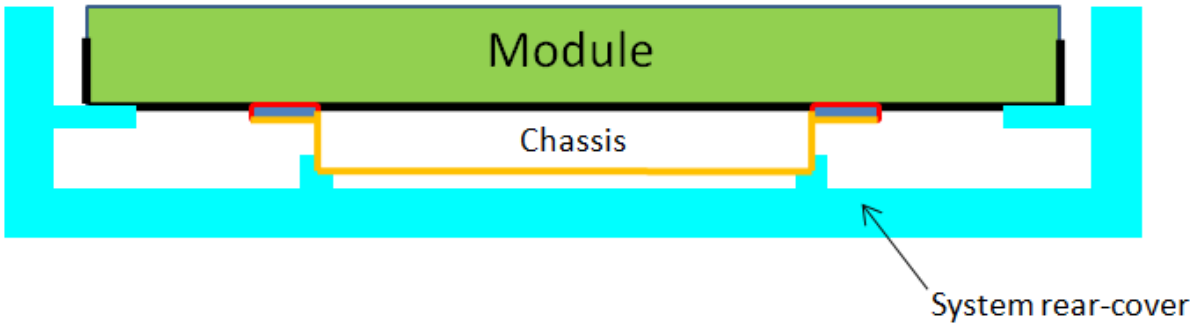
NOTES:  
 1. DISPLAY AREA POSITION TOLERANCE: |A-B|<=0.5mm & |C-D|<=0.5mm.  
 2. DISPLAY AREA POSITION TOLERANCE: |E-F|<=0.5mm.  
 3. (A) MARKS THE REFERENCE DIMENSION.  
 4. CONNECTOR TYPE: STM, NSAK2402SP, 30MB or I-PEX 20455-030E-76 OR EQUIVALENT.

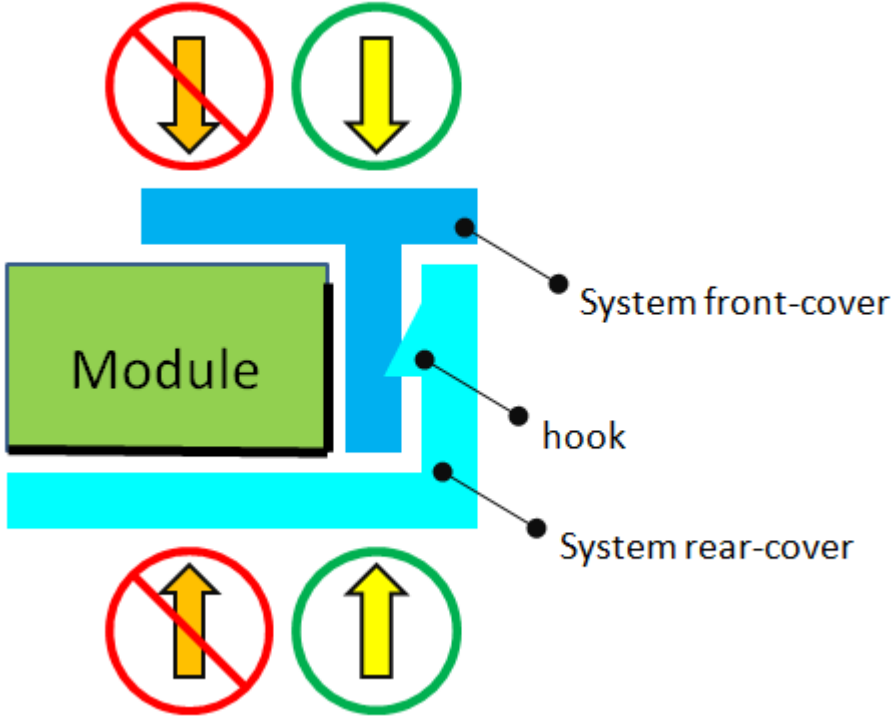
Appendix. SYSTEM COVER DESIGN NOTICE

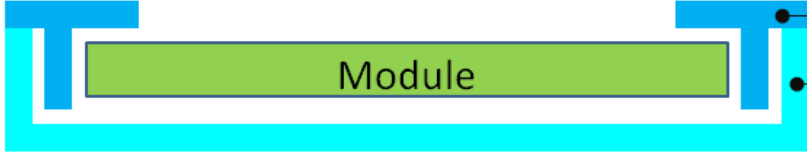
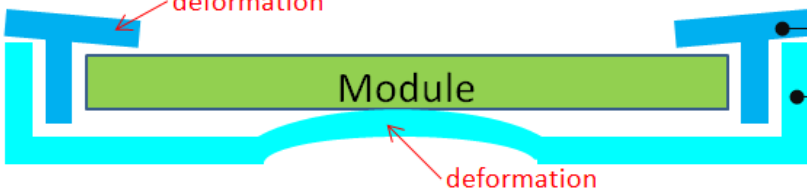
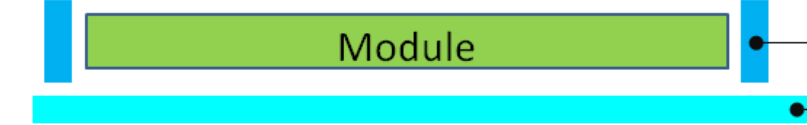
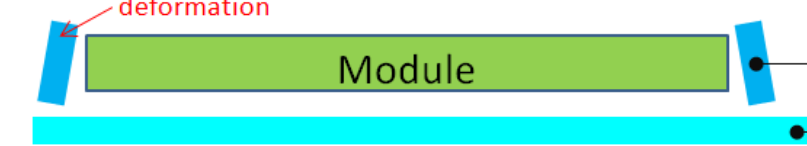
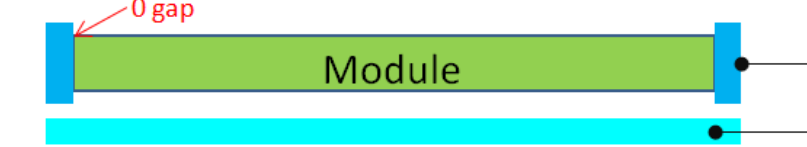
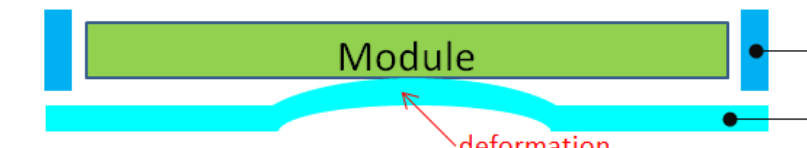
1	Set Chassis and IAVM Module touching Mode
	 <p>Module</p> <p>Chassis</p> <p>spring</p>
	 <p>Module</p> <p>Chassis</p> <p>Flat sheet metal</p>
	 <p>Module</p> <p>Chassis</p> <p>EMI Shielding Gasket (Tape/ Sponge)</p>
<p>Definition</p>	<p>a. To prevent from abnormal display &amp; white spot after mechanical test, it is not recommended to use spring type chassis.</p> <p>b. We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, second is Flat sheet metal type chassis.</p>

2	Tape/Sponge design on system inner surface
<p>The top diagram shows a cross-section of a Module (green) mounted on a Chassis (orange) with a System rear bezel (cyan). A layer of Tape/Sponge (red) is placed between the Module and the Chassis. Below this are two top-down views of the Module area. The first view, marked with a red 'X', shows four L-shaped pieces of Tape/Sponge placed at the corners of the Module. The second view, marked with a blue circle, shows a single rectangular piece of Tape/Sponge covering the entire area of the Module.</p>	
Definition	<p>a. To prevent from abnormal display &amp; white spot after mechanical test, we suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot.</p> <p>b. When using the Tape/Sponge, we suggest it be lay over between set chassis and Module rear cover. It is not recommended to add Tape/Sponge in separate location. Since each Tape/Sponge may act as pressure concentration location.</p>

3	<b>System inner surface examination</b>
	
Definition	<p>a. The hatch area on Module PCBA should keep at least 1mm gap(X,Y,Z direction) to any structure with system cover inner surface.</p> <p>b. Burr, Step, PCB protrusion may cause stress concentration. White spot may occur during reliability test.</p>

4	<b>Material used for system rear-cover</b>
	
Definition	<p>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss position for module's bracket are deformed open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</p>

5	Assembly SOP examination for system front-cover with hook structure
	
Definition	To prevent panel crack during system front-cover assembly process with hook structure, it is not recommended to press panel or any location that relate directly to the panel.

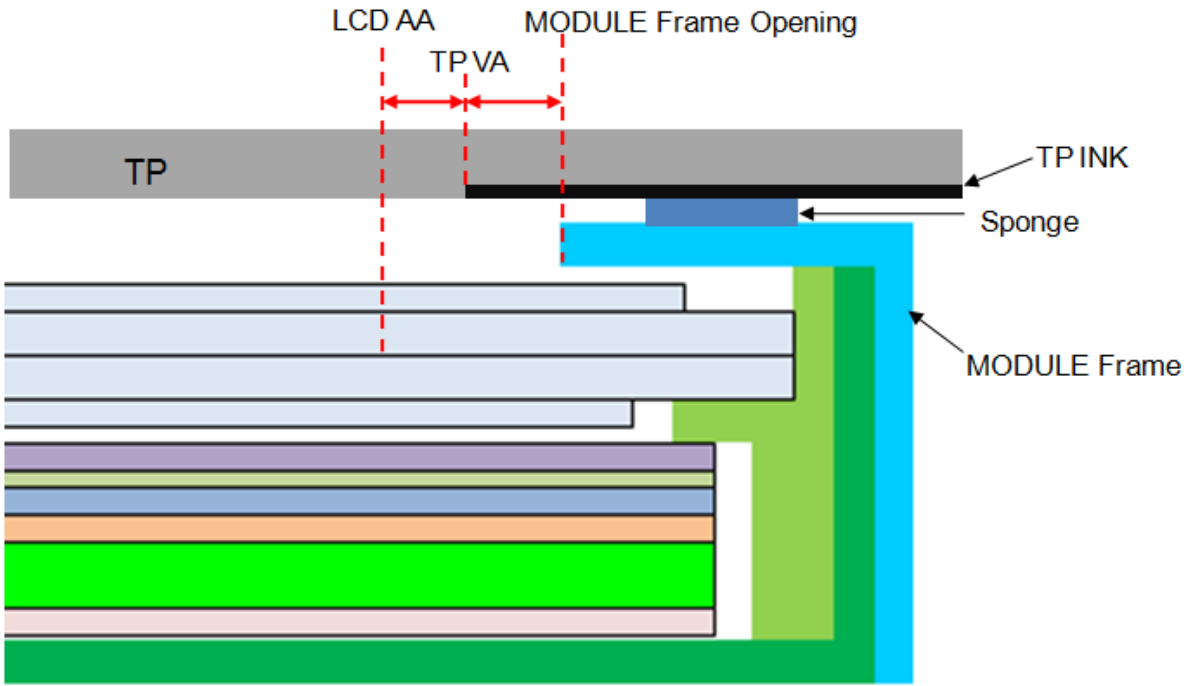
6	Permanent deformation of system cover after reliability test
○	 <p>● System front-cover ● System rear-cover</p>
✗	 <p>● System front-cover ● System rear-cover</p>
○	 <p>● System front-cover ● System rear-cover</p>
✗	 <p>● System front-cover ● System rear-cover</p>
✗	 <p>● System front-cover ● System rear-cover</p>
✗	 <p>● System front-cover ● System rear-cover</p>
Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell crack.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>



7	<b>Design gap A between panel &amp; any components on system rear-cover</b>
Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell crack.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

8	<b>Design gap B between system front-cover &amp; panel surface</b>
Definition	<p>Gap between system front-cover &amp; panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

9	Design gap C between panel & system front-cover or protrusions
Definition	<p>Gap between panel &amp; system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.</p> <p>The gap should be large enough to absorb the maximum displacement during the test.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

10	Design distance between TP AA to LCD AA
 <p>The diagram shows a cross-section of a display module. At the top is a grey layer labeled 'TP'. Below it is a black layer labeled 'TP INK'. Underneath the TP INK is a blue layer labeled 'Sponge'. Below the sponge is a green layer labeled 'MODULE Frame'. The LCD AA is shown as a stack of layers (light blue, purple, blue, orange, green, pink) below the TP and TP INK. The TP VA is indicated by a red double-headed arrow between two vertical dashed lines, one labeled 'LCD AA' and the other 'MODULE Frame Opening'. The TP INK is shown as a black layer extending from the TP layer towards the right, overlapping the TP VA area.</p>	
Definition	TP VA should avoid TP ink area covering LCD AA or causing the module frame to be exposed.

11	<b>Use OCR Lamination</b>
Definition	<ol style="list-style-type: none"> <li>1.OCR glue as possible beyond module, in order to avoid Line Pooling</li> <li>2.Add side glue to avoid Line Pooling</li> </ol>

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