DATA MODUL

Specification

S101ZWX89FP-FC86

10,1" - 1280*720 – LVDS

Spec Revision: 2.0
Revision Date: 07/02/2024

Note: This specification is subject to change without prior notice

Passion Displayed

PRODUCT SPECIFICATION

CDTECH Model: **S101ZWX89FP-FC86**

CUSTOMER Model: -

Description: **10.1 ” TFT-LCD Module with CTP**

Version: **2.0**

CDTECH	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE			
DATE	2024.7.2	2024.7.2	2024.7.2

	SIGNATURE	DATE
CUSTOMER APPROVAL		

Record of Revisions

Version	Revise Date	Description	Page
1.0	2024-6-19	First Release	-
	2024-6-21	Update TP-FPC shape	21
2.0	2024-7-2	Update Brightness	16

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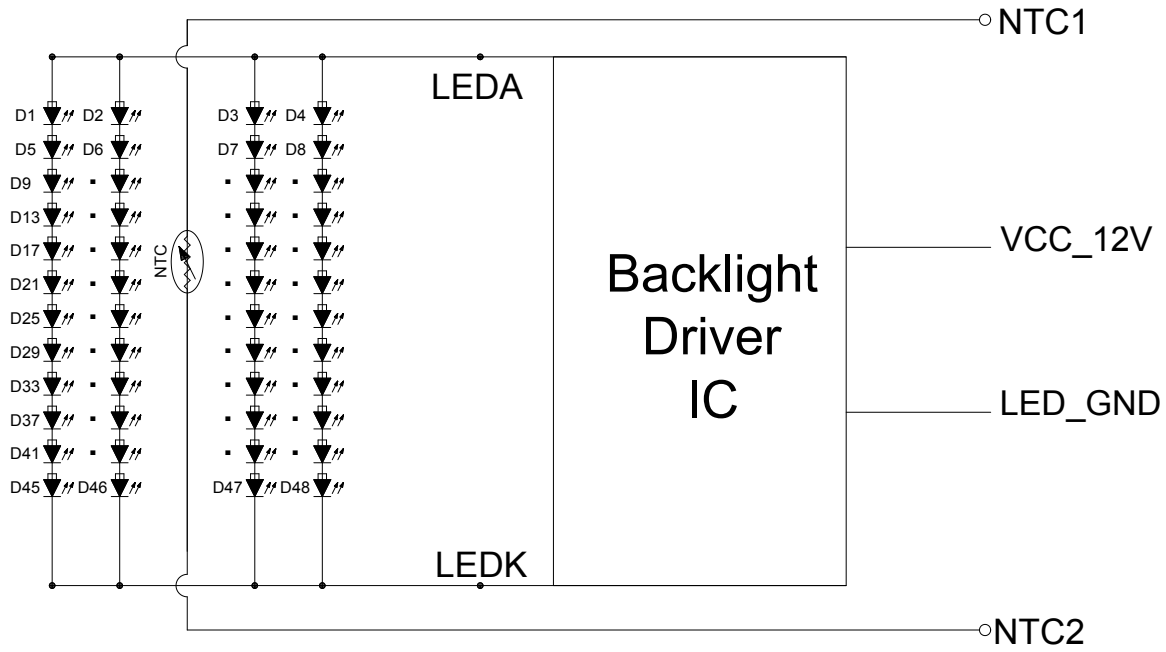
Note 2:LED circuit :



CIRCUIT DIAGRAM
VF =32.4~39.6V; IF=360mA

3.3 Touch Panel (I2C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	I2C_VDD 3.3V	-	3.3	-	V	
Analog supply current	$I_{I2C\_VDD\ 3.3V}$	-	TBD	-	mA	I2C_VDD 3.3V =3.3V
Input high-level voltage	VIH	0.7*I2C_VDD 3.3V	-	I2C_VDD 3.3V	V	
Input low -level voltage	VIL	GND	-	0.3*I2C_VD D 3.3V	V	

3.4 Touch Panel (USB)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply voltage	USB_VDD 5V	-	5.0	-	V	
Analog supply current	$I_{USB\_VDD\ 5V}$	-	TBD	-	mA	USB_VDD 5V =5.0V
Input high-level voltage	VIH	0.7*USB_VDD 5V	-	USB_VDD 5V	V	
Input low -level voltage	VIL	GND	-	0.3*USB_VDD 5V	V	

4.2 Touch FPC Pin Assignment (CN1 Connector：SM06B-SRSS-TB (side entry type))

No.	Symbol	Description
1	USB_VDD (5V)	Power supply for CTP (5V)
2	USB_D-	Data- input
3	USB_D+	Data+ input
4	USB_GND	Ground

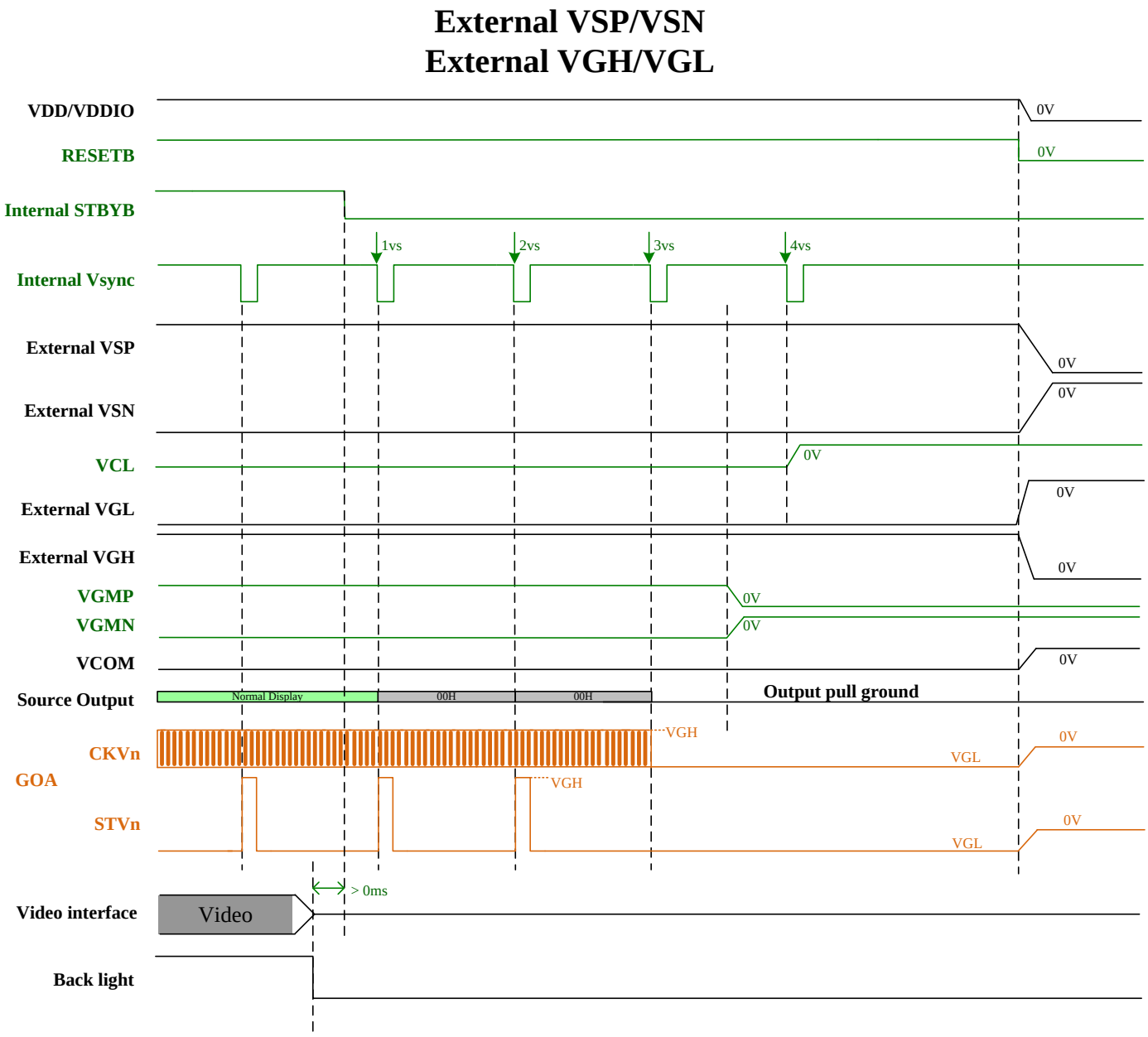
4.3 Touch FPC Pin Assignment (CN2 Connector：JST SM04B-SRSS-TB)

No.	Symbol	Description
1	I2C_GND	Ground
2	I2C_VDD 3.3V	Power supply for CTP (3.3V)
3	I2C_RST	Reset Pin for CTP
4	I2C_SCL	I2C clock input for CTP
5	I2C_INT	Interrupt signal for CTP
6	I2C _SDA	I2C data input and output for CTP

4.3 Touch FPC Pin Assignment (CN3 Recommended Connector：FH12-10S-0.5SH(55))

No.	Symbol	Description
1	USB_GND	Ground
2	USB_VDD (5V)	Power supply for CTP (5.0V)
3	USB D-	Data- input
4	USB D+	Data+ input
5	I2C_GND	Ground
6	I2C_VDD (3.3V)	Power supply for CTP (3.3V)
7	I2C_RST	Reset Pin for CTP
8	I2C_SCL	I2C clock input for CTP
9	I2C_INT	Interrupt signal for CTP
10	I2C _SDA	I2C data input and output for CTP

Power off sequence



5.2 AC Characteristics

LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	30	-	TBD	MHz	Refer to input timing table for each display resolution
Input data skew margin	T_{RSKM}	500	-	-	ps	|VID| = 200mV RxVCM = 1.2V RxFCLK = 81MHz
Clock high time	T_{LVCH}	-	4/(7* R_{xFCLK})	-	ns	
Clock low time	T_{LVCL}	-	3/(7* R_{xFCLK})	-	ns	
PLL wake-up time	T_{enPLL}	-	-	150	us	

Table 13.1: LVDS mode AC electrical characteristics

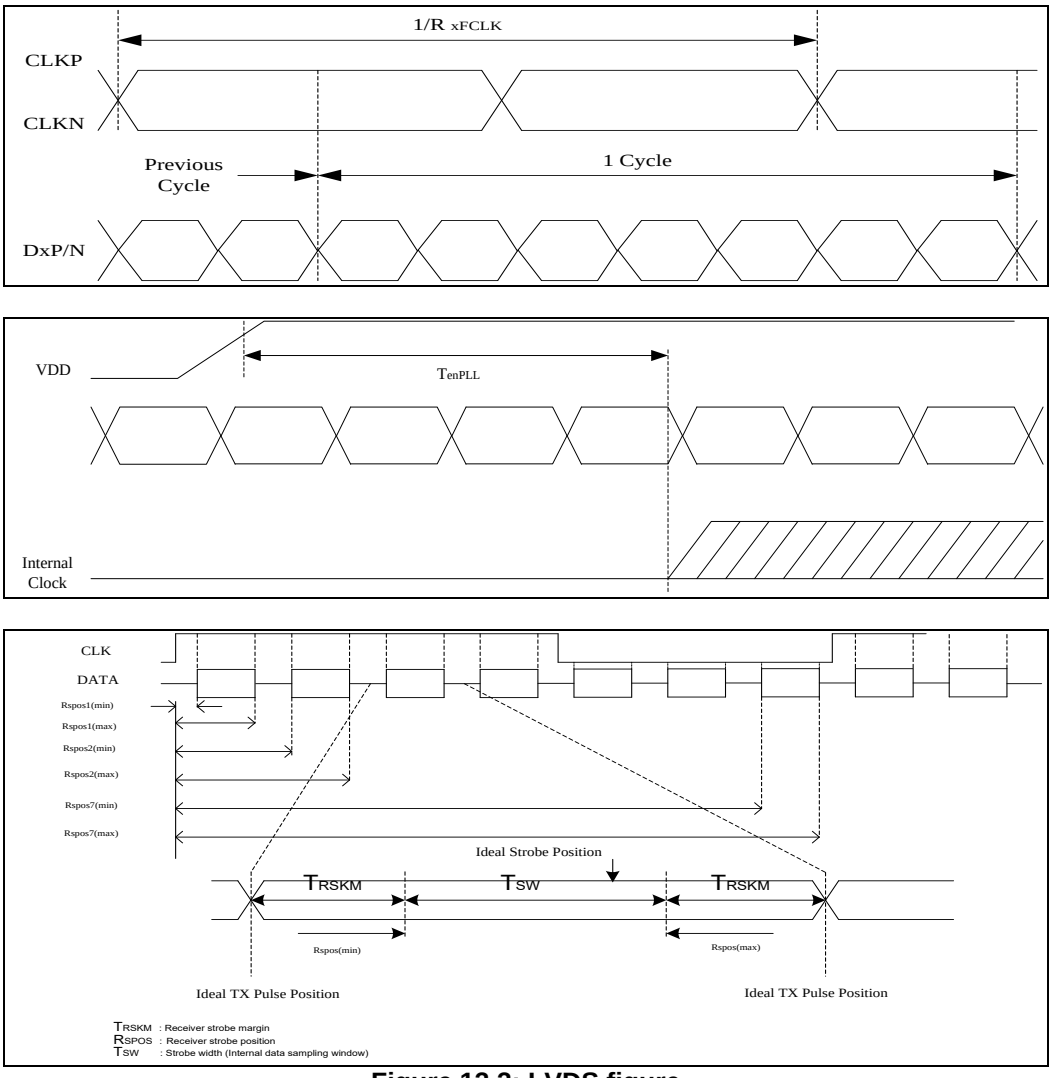


Figure 13.3: LVDS figure

Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(Test condition: VDDIO=2.3V~3.6V, VSS=0V, T_A=-30 ~+85)

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		20	-	-	μs

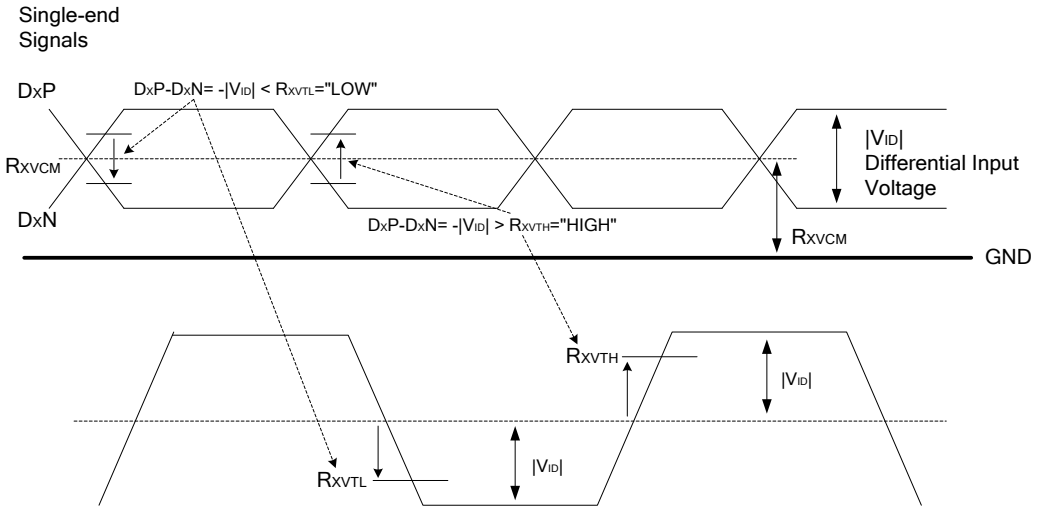
Figure 13.5: Reset timing

5.3 DC Characteristics

LVDS DC electrical characteristics

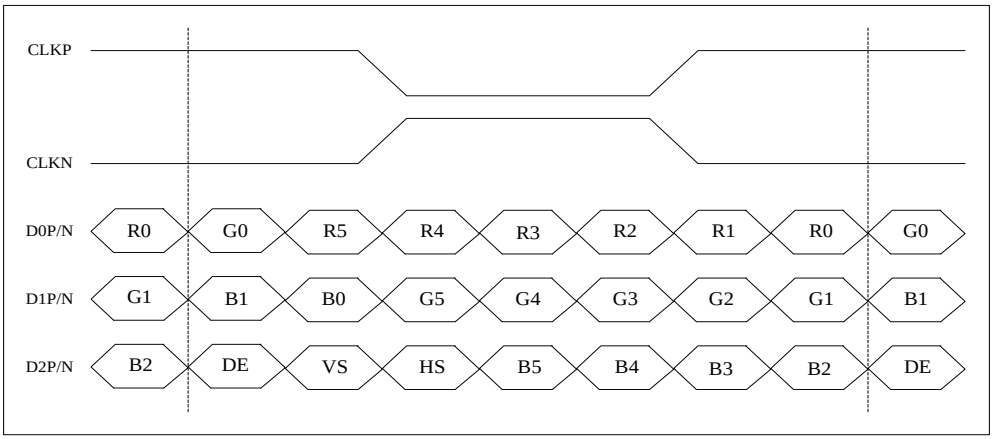
(VDD=VDDIO=VDDIF=2.3 to 3.6V, VSS=VSSA=VSS_IF=0V, TA=-30 to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential input high threshold voltage	R_{XVTH}	-	-	+0.1	V	R_{XVCM}=1.2V
Differential input low threshold voltage	R_{XVTL}	-0.1	-	-	V	
Input voltage range (singled-end)	R_{XVIN}	0.7	-	1.7	V	
Differential input common mode voltage	R_{XVCM}	1	1.2	1.4	V	$\|V_{ID}\|$=0.2
Differential input impedance	Z_{ID}	80	100	125	ohm	
Differential input voltage	$\|V_{ID}\|$	0.2	-	0.6	V	
Differential input leakage current	I_{LCLVDS}	-10	-	+10	uA	
LVDS Digital Operating Current	I_{VDD}	-	15	20	mA	F_{DCLK}=80MHz,VDD=3.3V, Input pattern: 55h->Aah->55h->Aah
LVDS Digital Stand-by Current	I_{ST}	-	-	250	uA	Clock & all Functions are stopped

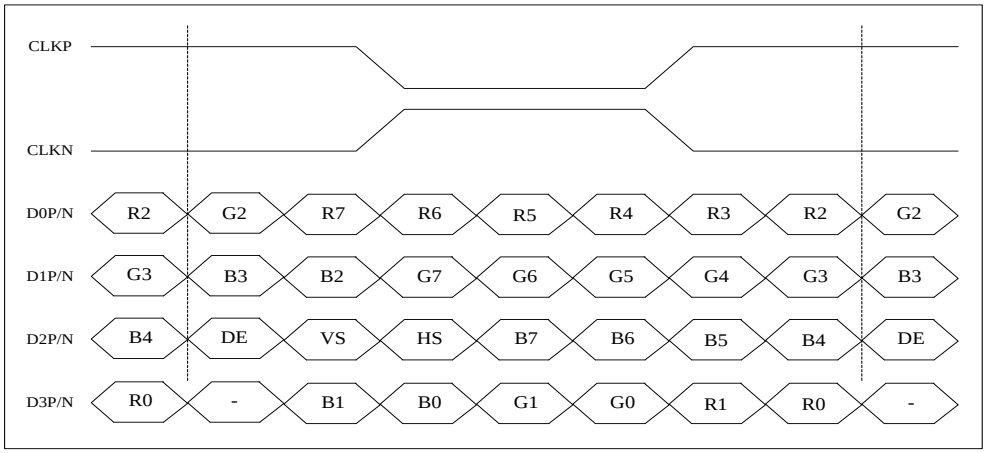


5.4 LVDS interface

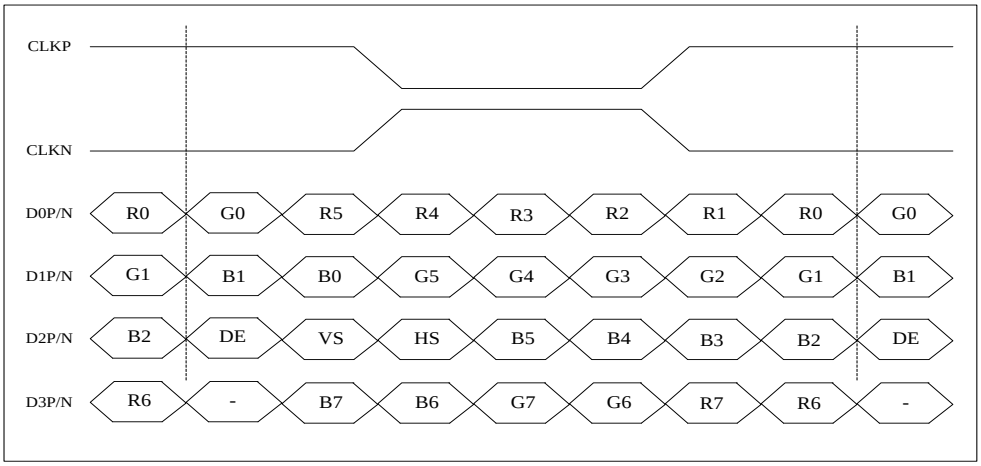
Data input format for LVDS



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



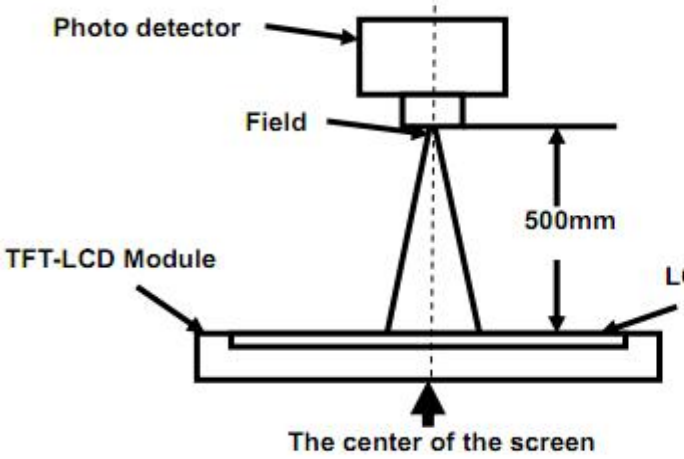
8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input(LVBIT=H, LVFMT=H)

For 1280RGBx720

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	61.6	65.5	71.3	MHz
HSYNC period time		T_H	1380	1440	1500	DCLK
Horizontal display area		T_{HD}	1280			DCLK
HSYNC pulse width	Min.	T_{HPW}	2			
	Typ.		-			
	Max.		40			
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	12	72	132	DCLK
VSYNC period time		T_V	744	758	792	H
Vertical display area		T_{VD}	720			H
VSYNC pulse width	Min.	T_{VPW}	2			H
	Typ.		-			
	Max.		20			
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Fig 1

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

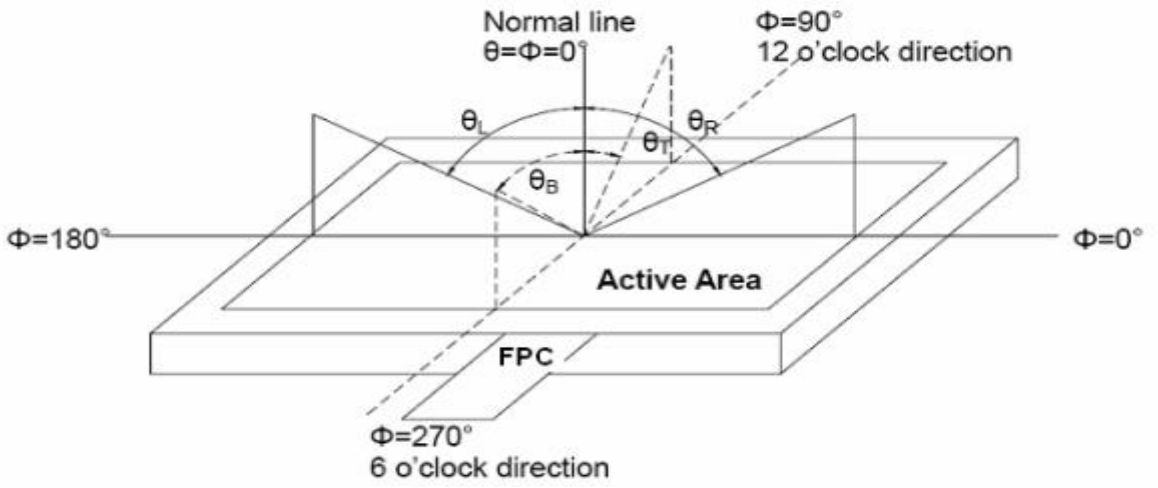


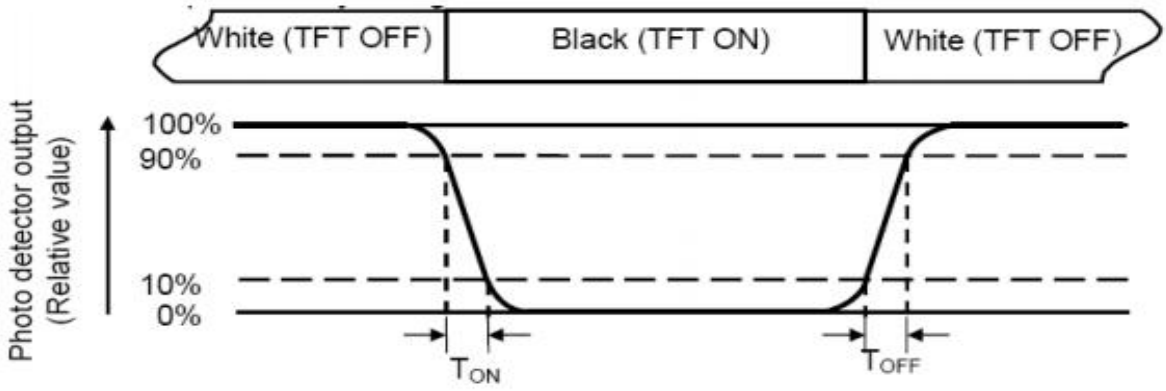
Fig 2 Definition of viewing angle

Note 3: Definition of contrast ratio

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.3-a/b

Note 7:Surface luminance is the luminance with all pixels displaying white.

Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

For more information see FIG.3-a/b

Note 8:Size : S≤5”(see Figure a) A : 5 mm B : 5 mm. H,V : Active area

Light spot size ⌀ =5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or test spot position : see Figure a.

measurement instrument : TOPCON’s luminance meter SR-3A or BM-7 or compatible (see Figure 1).

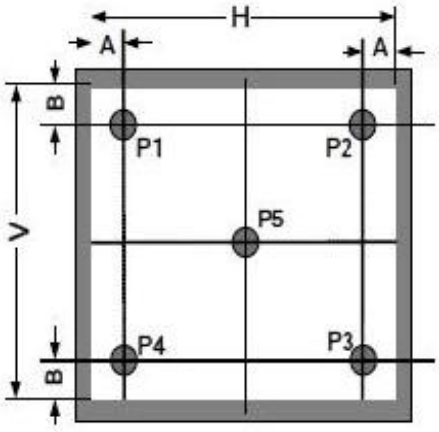


Fig. 3-a Definition of points

5”＜S≤12.3”(see Figure b) . H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens. test spot position : see Figure b.
measurement instrument : TOPCON’s luminance meter SR-3A or BM-7 or compatible (see Figure 1).

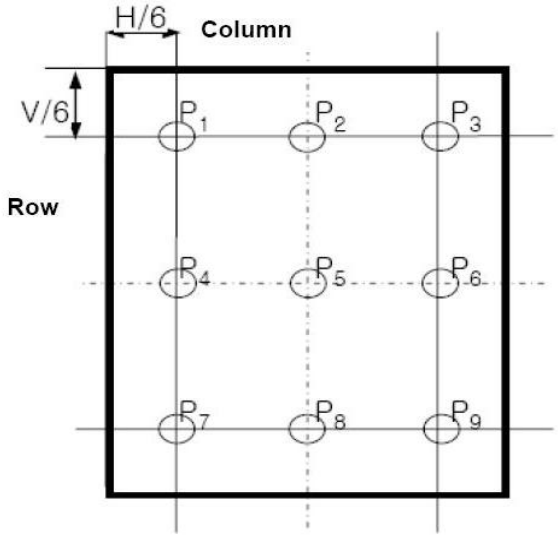


Fig. 3-b Definition of points

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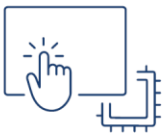
Passion Displayed



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