

- Tentative Specification
- Preliminary Specification
- Approval Specification

MODEL NO.: S315DJ1

SUFFIX: A01

Revision : B3	
Customer :	
APPROVED BY	SIGNATURE
Name / Title _____	
Note	

Please return 1 copy for your confirmation with your signature and comments.	

Approved By	Checked By	Prepared By
Chris Chen	John Hsieh	Chiawen Chen

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 1.0	2024. 8. 28	ALL	ALL	Preliminary Specification first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

S315DJ1-A01 is a 31.5" TFT Liquid Crystal Display PID module with LED Backlight unit and 4 lane-eDP interface. This module supports 3840 x 2160 Quad Full HDTV format and can display true 1.07G colors (8-bit+FRC). The driving board module for backlight is built-in.

1.2 FEATURES

- Brightness 500 nits
- Contrast ratio 1000:1
- Fast response time Gray to gray average 14 ms
- High color saturation DCI-P3 95%
- Quad Full HDTV (3840 x 2160 pixels) resolution, Quad Full HDTV format
- eDP interface
- Optimized response time for 50Hz/60Hz frame rate
- Ultra wide viewing angle : AAS technology
- Viewing Angle : 178(H)/178(V) (CR ≥ 10) AAS Technology
- RoHs compliance
- T-con input frame rate: 50Hz/60Hz, output frame rate: 50Hz/60Hz

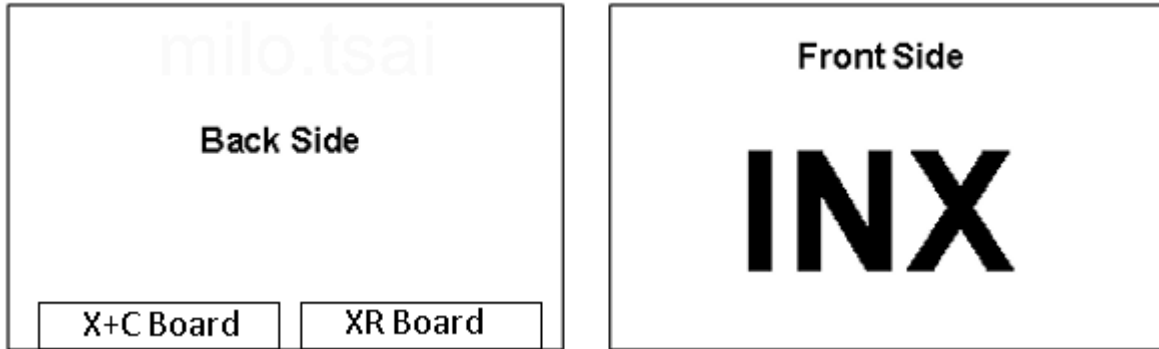
1.3 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	697.3056 (H) x 392.2344 (V) (31.5" diagonal)	mm	(1)
Bezel Opening Area	701.4(H) x 396.2(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840 x R.G.B. x 2180	pixel	-
Pixel Pitch	0.18(H) x 0.18(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.073G (8-bit+ Hi-FRC)	color	-
Display Operation Mode	AAS, Normally black	-	-
Surface Treatment	AG type, 3H hard coating, Haze 25	-	(2)
Rotation Function	Unachievable		(3)
Display Orientation	Signal input with "INX"		(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. INX reserves the rights to change this feature.

Note (3)



1.4 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	715.2	716.2	717.2	mm	(1)
	Vertical (V)	415.2	416.2	417.2	mm	(1)
	Thickness (T)	13.7	14.7	15.7	mm	(2)
	Thickness (T)	20.4	21.4	22.4	mm	(3)
Weight		3000	3200	3400	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to Converter cover

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

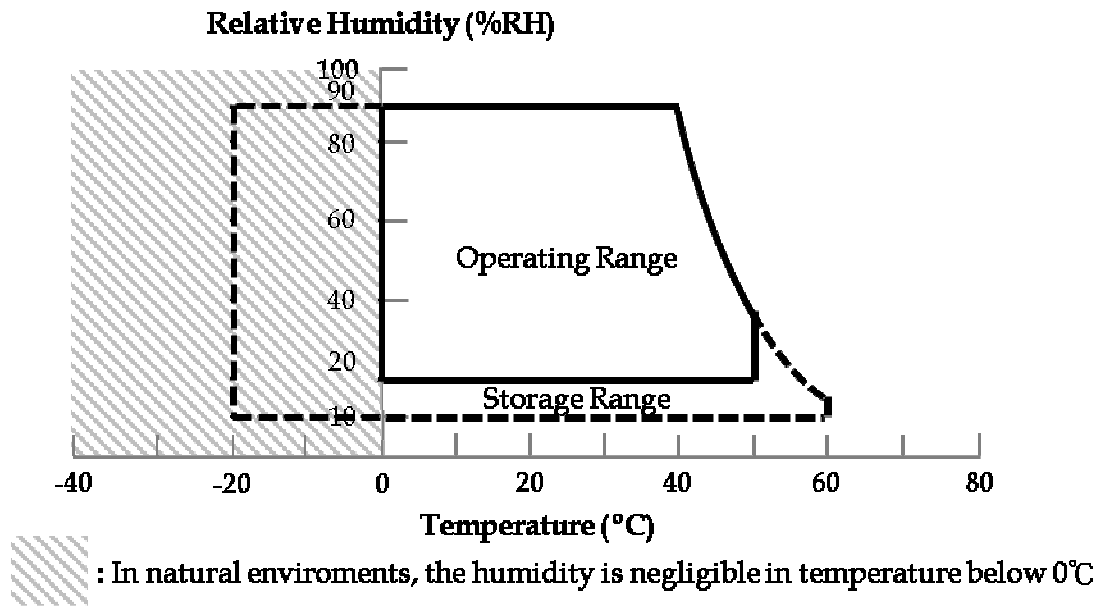
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1), (3), (4)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (3), (4)
Panel Surface Temperature	T _{PS}	-	+65	°C	(2)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. (Ta ≤ 40 °C).
- (b) Wet-bulb temperature should be 39 °C Max.
- (c) No condensation.

Note (2) Surface temperature is measured at 50 °C dry condition.

Note (3) The specified temperature range is determined by the design of the product module. When integrated with the customer’s system, it is imperative to control environmental conditions within this prescribed range; otherwise, the operational capability of the product cannot be guaranteed.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Light Bar Voltage	VW	—	62.5	VRMS	
Converter Input Voltage	VBL	21.6	26.4	V	(1)
Control Signal Level	—	-0.3	6	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

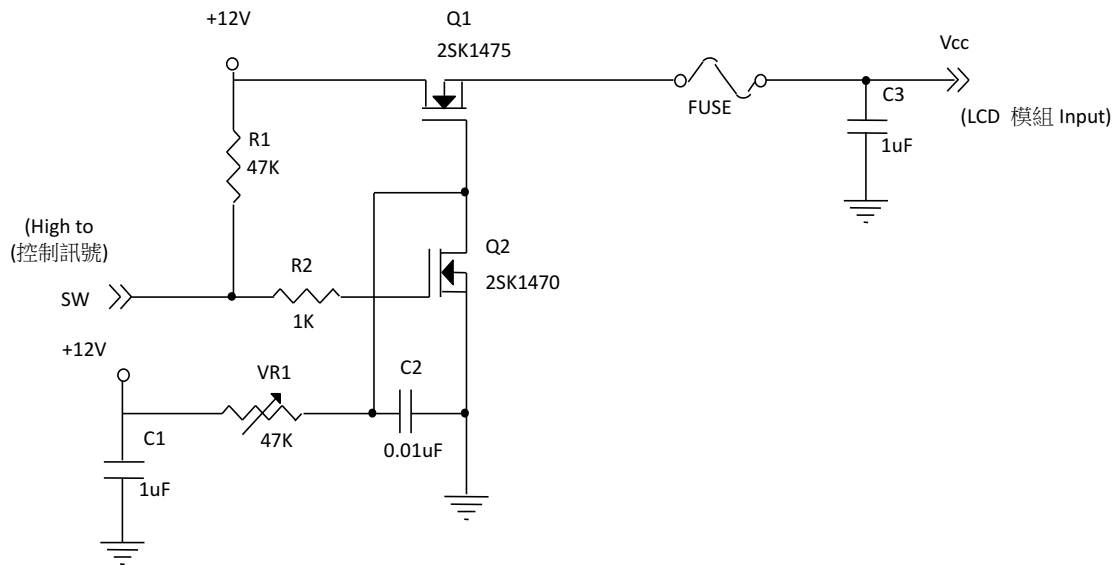
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

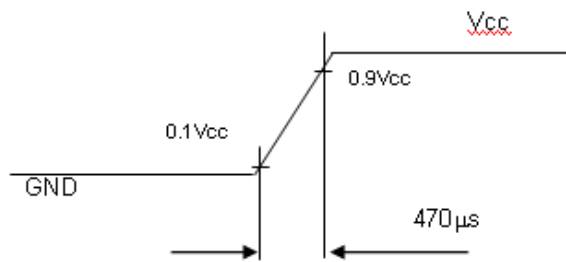
Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Power Supply Voltage	V _{CC}	10.8	12	13.2	V		
Ripple Voltage	V _{RP}	-	-	300	mV		
Rush Current	I _{RUSH}	-	-	3	A	(2)	
Power Supply Current	White	I _{CC}	-	(0.53)	(0.58)	A	(3a)
	Black		-	(0.48)	(0.53)	A	(3b)
	Max Power Pattern		-	(0.9)	(0.98)	A	(3c)
Power Consumption	Typ. FR	PLCD	-	(10.82)	(11.81)	Watt	(4)
	Max. FR		-	(11.28)	(12.30)	Watt	
eDP interface	Differential peak to peak voltage	V _{dp-p}	120	-	1320	mV	
	DC common mode voltage		0	-	2	V	
	Differential Input Resistor	RRIN	80	100	120	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	
	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	

Note (1) The ambient temperature is Ta = 25 ± 2 °C.

Note (2) Measurement Conditions:



Vcc rising time is 470μs



Note (3) The specified power supply current is under the conditions at $V_{cc} = 12V$, $T_a = 25 \pm 2^\circ C$, $F_r = 60Hz$, whereas a power dissipation check pattern below is displayed.

a. White Pattern↵



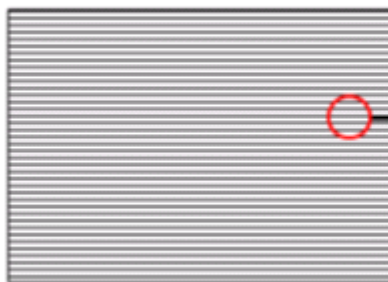
Active Area↵

b. Black Pattern↵



Active Area↵

c. Horizontal Pattern↵

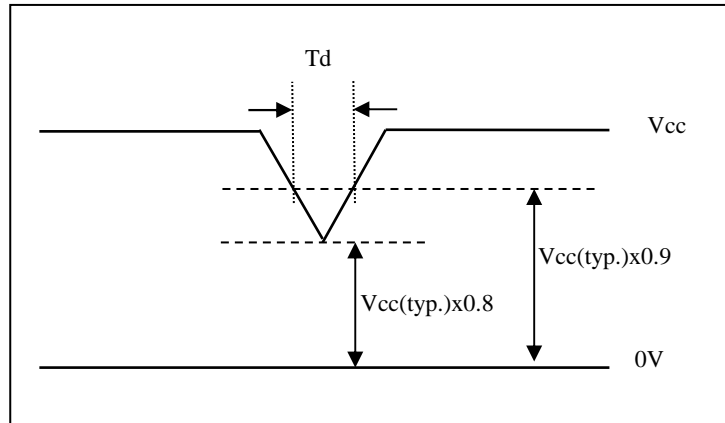


Active Area↵



Note (4) The power consumption is specified at the pattern with the maximum current

3.2 VCC POWER DIP CONDITION



Dip condition: $9.6 \leq V_{cc} \leq 10.8$, $T_d \leq 20\text{ms}$

3.3 BACKLIGHT CONVERTER UNIT

3.3.1 CONVERTER CHARACTERISTICS (Ta=25±2°C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	27	32	W	(1), (2)
Converter Input Voltage	V _{BL}	22.8	24	25.2	VDC	
Converter Input Current	I _{BL}	-	1.13	1.35	A	Non Dimming
Input Inrush Current	I _R	-	-	6.7	A _{peak}	V _{BL} =22.8V _r (3), (6)
Dimming Frequency	FB	150	-	170	Hz	(5)
Dimming Duty Ratio	DDR	5	-	100	%	(4), (5)
Life Time	-	50000	-	-	Hrs	(7)

Note (1) The power supply capacity should be higher than the total converter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 31.5" backlight unit under input voltage 24V.

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 20ms.

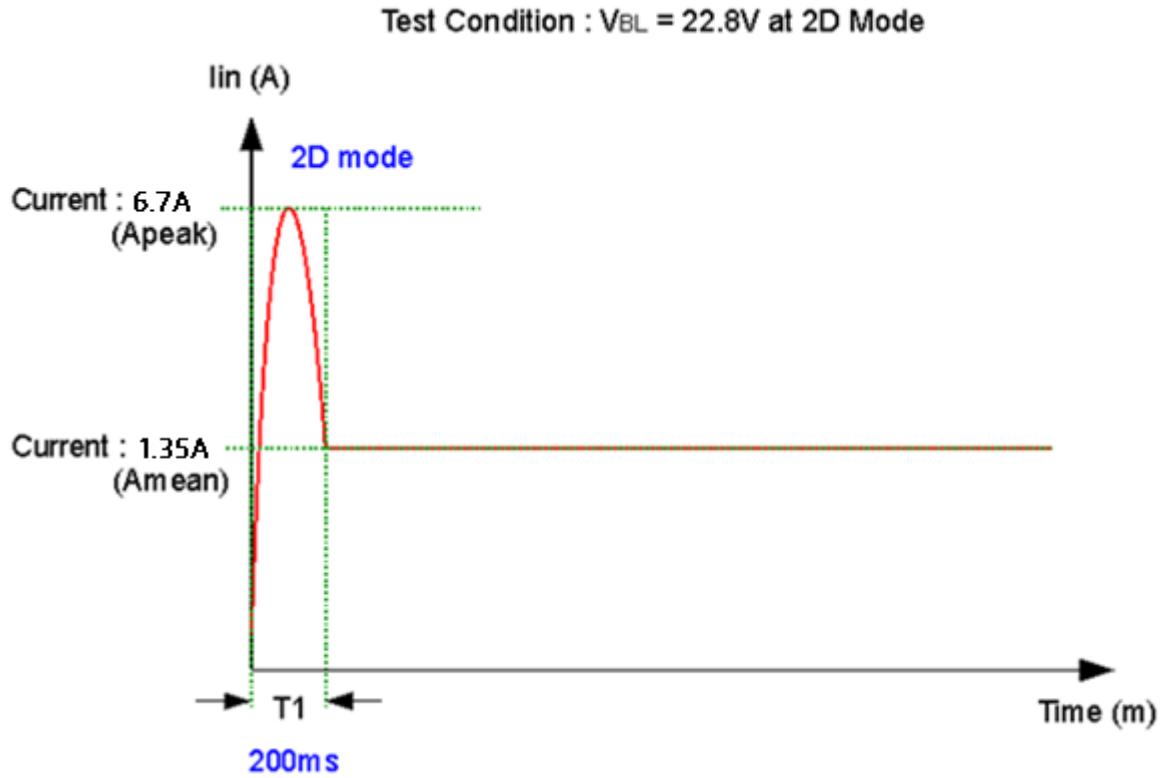
Note (4) EPWM signal have to input available duty range. 5% minimum duty ratio is only valid for electrical operation.

Note (5) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value,

Operating condition: Continuous operating at Ta = 25±2°C

Note (6) Below diagram is only for power supply design reference.

Note (7) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value,
Operating condition: Continuous operating at $T_a = 25 \pm 2^\circ\text{C}$



3.3.2 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on	(5)
	LO		—	0	—	0.8	V	Duty off	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector	
VBL Rising Time		Tr1	—	20	—	—	ms	10%-90% V _{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us		
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ		
PWM Delay Time		TPWM	—	100	—	—	ms		
BLON Delay Time		T _{on}	—	300	—	—	ms		
		T _{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

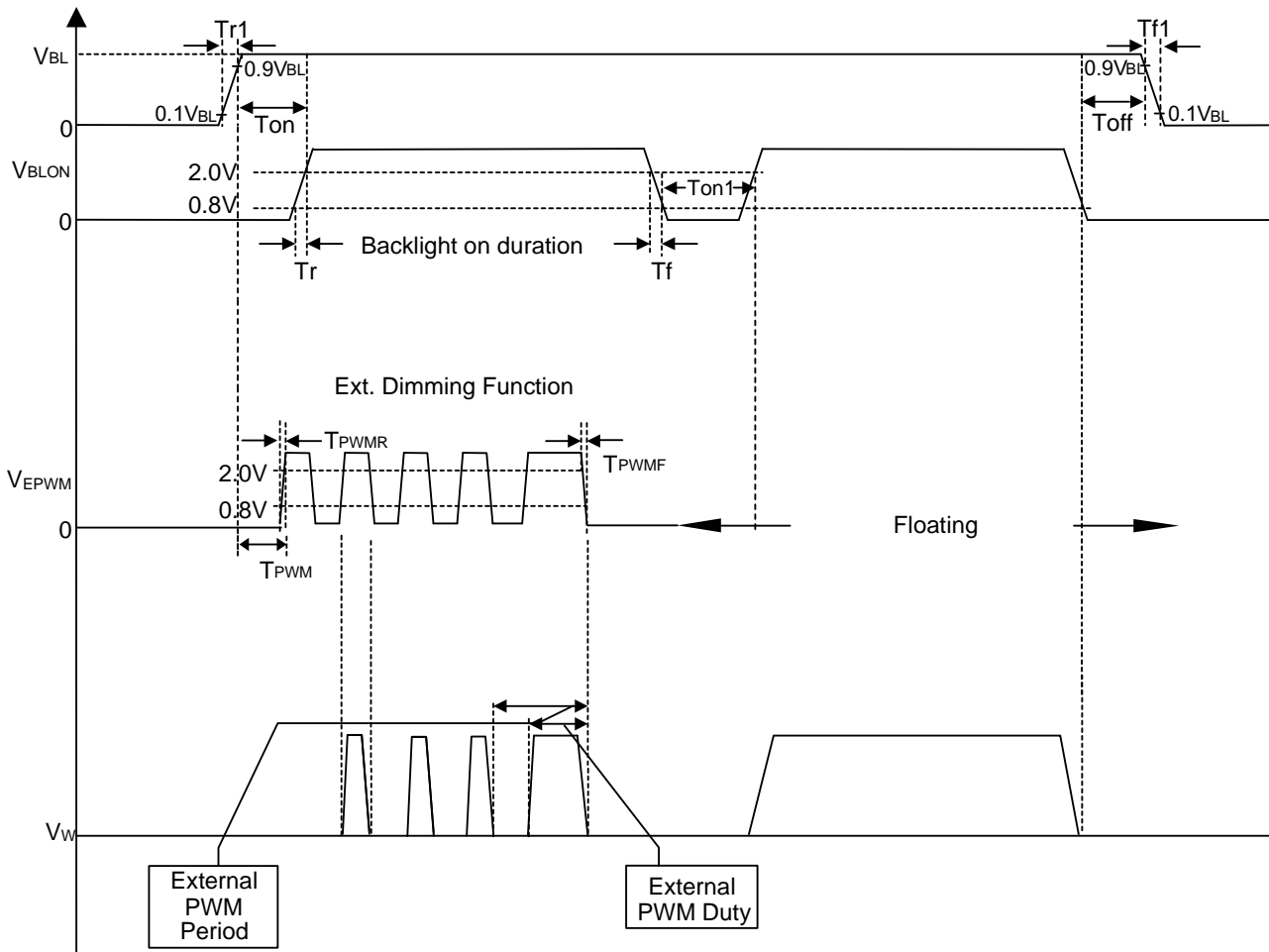
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. (Fig.2)

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

Note (6) EPWM signal have to input available frequency range.



100%

Fig. 1

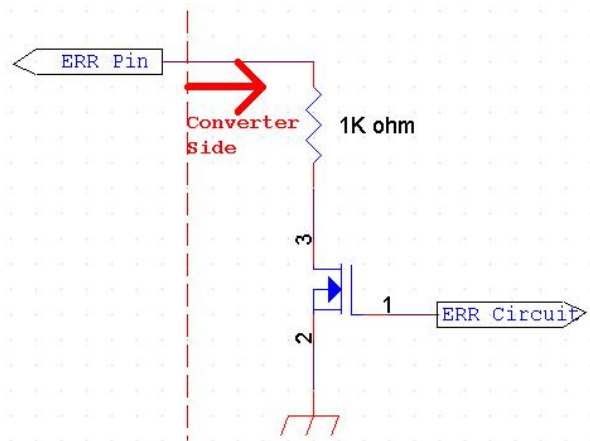


Fig. 2

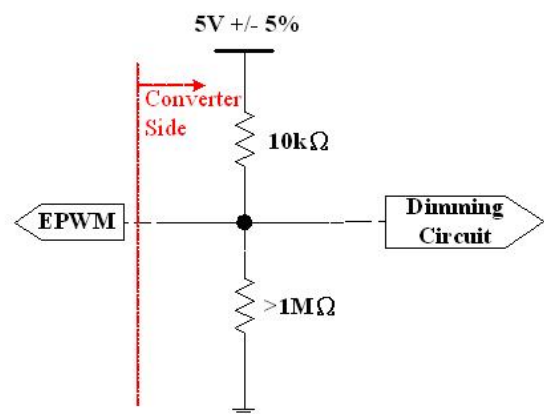


Fig. 3

4. INTERFACE PIN CONNECTION

4.1 TFT LCD MODULE

Pin	Name	Description	Note
1	Vin	Power input (+12V)	
2	Vin	Power input (+12V)	
3	Vin	Power input (+12V)	
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	
6	Vin	Power input (+12V)	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	
11	N.C.	No Connection	
12	GND.	Ground	
13	N.C.	No Connection	
14	N.C.	No Connection	
15	N.C.	No Connection	
16	GND.	Ground	
17	GND.	Ground	
18	RX0P	True Signal for Main Link 0	
19	RX0N	Component Signal for Main Link 0	
20	GND.	Ground	
21	RX1P	True Signal for Main Link 1	
22	RX1N	Component Signal for Main Link 1	
23	GND.	Ground	
24	RX2P	True Signal for Main Link 2	
25	RX2N	Component Signal for Main Link 2	
26	GND.	Ground	
27	RX3P	True Signal for Main Link 3	
28	RX3N	Component Signal for Main Link 3	
29	GND.	Ground	
30	AUXN	Component Signal for Auxiliary Channel	
31	AUXP	True Signal for Auxiliary Channel	
32	GND.	Ground	
33	HPD	Hot Plug Detect Signal	
34	GND.	Ground	
35	N.C.	No Connection	
36	GND.	Ground	
37	N.C.	No Connection	

38	N.C.	No Connection	
39	GND.	Ground	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	GND.	Ground	
43	N.C.	No Connection	
44	N.C.	No Connection	
45	GND.	Ground	
46	N.C.	No Connection	
47	N.C.	No Connection	
48	GND.	Ground	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	GND.	Ground	

Connector Information

Item	Description
Manufacturer	P-TWO or JAE
Type part number	187059-51221 (P-TW0) or FI-RE51S-HF (JAE)
User's Mating housing part number	P-Two LVDS 28 type_187120-51001-3 or JAE FI-RE51CL or Hamburg FCC-W50-510001-000C or compatible

4.2 BACKLIGHT UNIT

4.2.1 LIGHT BAR UNIT

[1] Connector (wire type)

Item	Description
Type part number	Cvilux CI1406M1VL0-N-NH ACES 50429-0060N-001 CJELE A126H-4400603S-R12

The pin configuration for the housing and lead wire is shown in the table below.

CNL01 · CNL02 Connector Pin Assignment:

CNL01

Pin No	Symbol	Feature
1	N1	Negative of LED String
2	N2	
3	N3	
4	VLED+	Positive of LED String
5	VLED+	
6	VLED+	

CNL02

Pin No	Symbol	Feature
1	VLED+	Positive of LED String
2	VLED+	
3	VLED+	
4	N4	Negative of LED String
5	N5	
6	N6	

4.2.2 CONVERTER UNIT

[1] Connector (wire type)

Item	Description
Type part number	Cvilux CI0114M1HR0-LA FCN JH2-D4-143N
Mating housing part number	Cvilux_CI0114S0000 or compatible

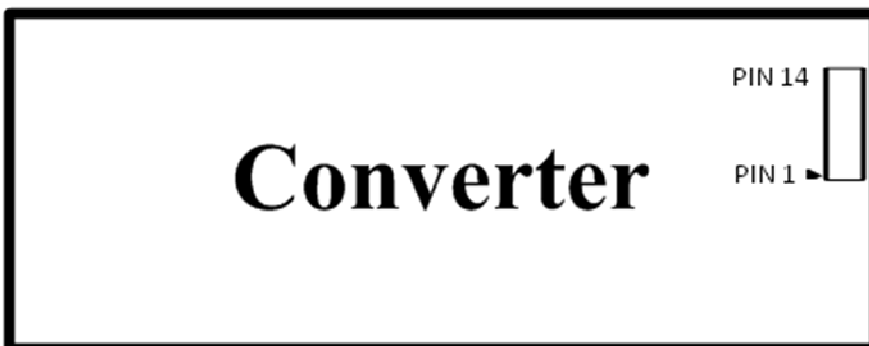
CNV04 Connector Pin Assignment:

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) ; Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Note (1) The pin14 must be connected to EPWM simultaneously.

Note (2) If Pin14 is open, E_PWM is 100% duty.

Note (3) Input connector pin order defined as follows



Input Connector

4.3 COLOR DATA INPUT ASSIGNMENT

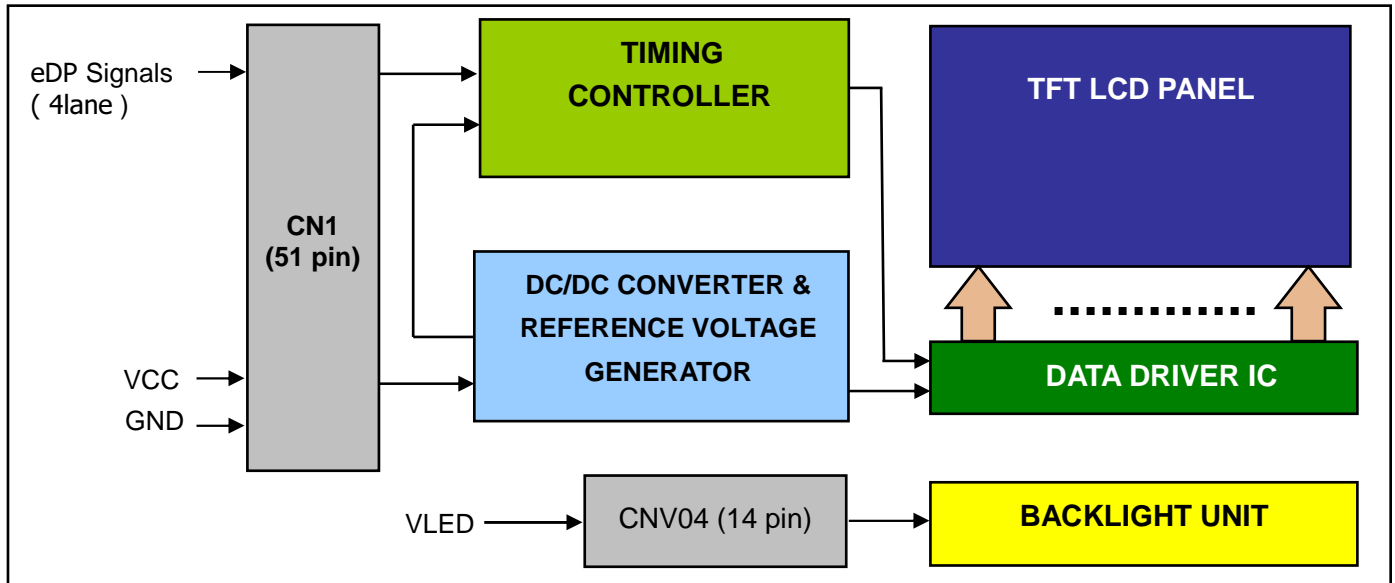
The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																											
		Red										Green										Blue							
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
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	Red(253)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(254)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red(255)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	Green(2)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
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	:	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	
	Green(253)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	Green(254)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
	Green(255)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5. ELECTRICAL SPECIFICATIONS

5.1 FUNCTION BLOCK DIAGRAM



5.2 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
eDP	Frequency	Fc	480	533.28	560	MHz	(1)
Vertical Display Term	Frame Rate	Fr	40	60	62.5	Hz	
	Total	Tv	2200	2222	3520	Th	Tv=Tvd+Tvb
	Active Display	Tvd	2160	2160	2160	Th	-
	Blank	Tvb	40	62	1360	Th	-
Horizontal Display Term	Horizontal Frequency	Fh	120.6	133.2	140.7	KHz	
	Total	Th	3980	4000	4020	Tc	Th=Thd+Thb
	Active Display	Thd	3840	3840	3840	Tc	-
	Blank	Thb	140	160	180	Tc	-

Note(1): In Free-sync mode, only guaranteed no functional failure, but don't guaranteed its quality of the optical and cosmetic performance.

Note(2): The optimal Vertical Frame Rate is 59~62.5Hz for best picture quality.

Note(3): Because this module is operated by DE only mode, Hsync and Vsync input signals are ignored.

$$F_c = F_r \times T_v \times T_h,$$

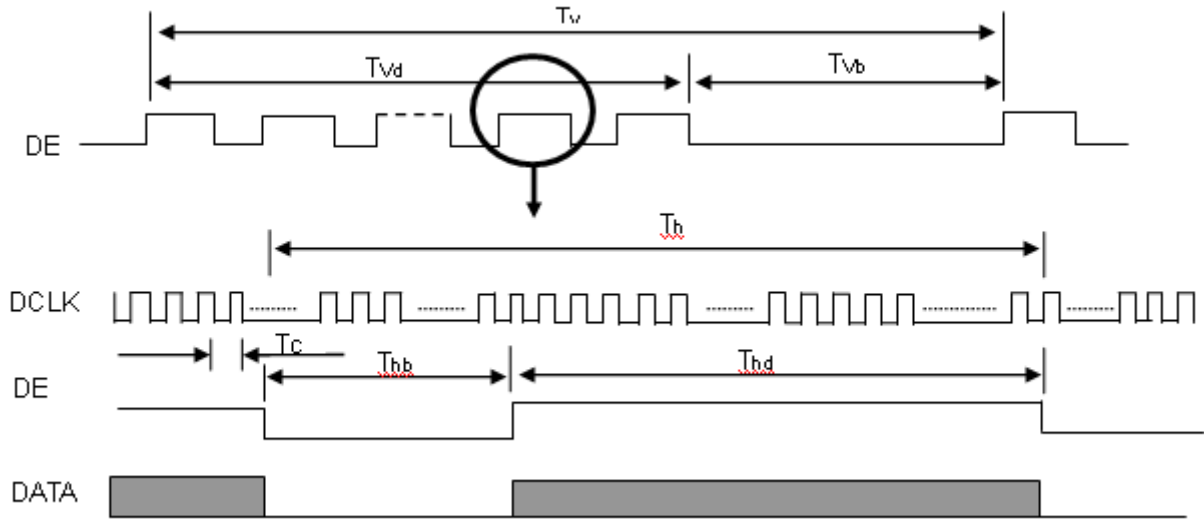
$$F_h(\text{min.}) = F_c(\text{min.}) / T_h(\text{min.}),$$

$$F_h(\text{typ.}) = F_c(\text{typ.}) / T_h(\text{typ.}),$$

$$F_h(\text{max.}) = F_c(\text{max.}) / T_h(\text{min.})$$

Please make sure the range of pixel clock has follow the below equation and F_c , F_r , T_v , T_h not allowed to get beyond the min or max spec.

INPUT SIGNAL TIMING DIAGRAM

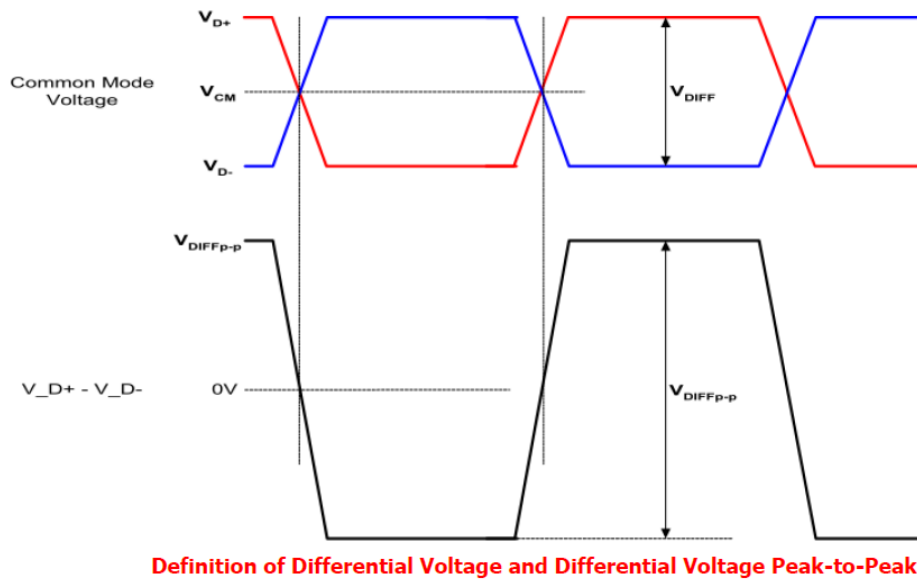


5.3. eDP SIGNAL SPECIFICATIONS

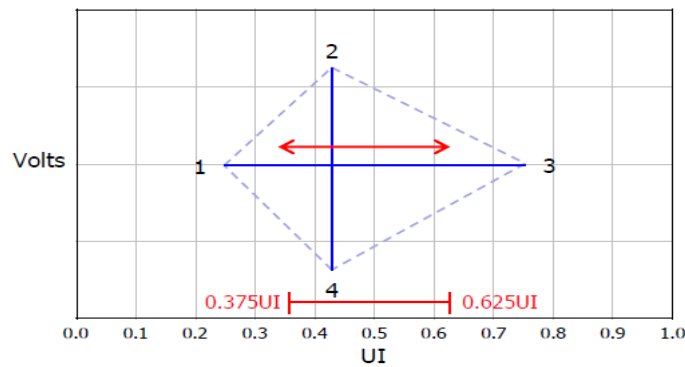
5.3.1 eDP MAIN LINK SIGNAL

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Frequency for high bit rate (HBR2)	fHBR2	-	5.4	-	Gbps	
Spread spectrum clock (Down Spreading)		0		0.5	%	(6)
SSC modulation frequency	fssc	30		33	kHz	(6)
Differential peak to peak voltage at RX connector	VRX-Diff p-p	120	-	1320	mV	(1)
Rx input DC common mode voltage	VCM	0	-	2	V	(1)
Differential termination resistance	VRX-TERM	80	100	120	ohm	
Rx intra-pair skew at HBR2	tTOSK_Intra	-	-	50	ps	(3)
Rx inter-pair skew at HBR2	tTOSK_Inter	-(4UI+500ps)	-	(4UI+500ps)	ps	(4)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(5)

Note(1) Definition of Differential Voltage



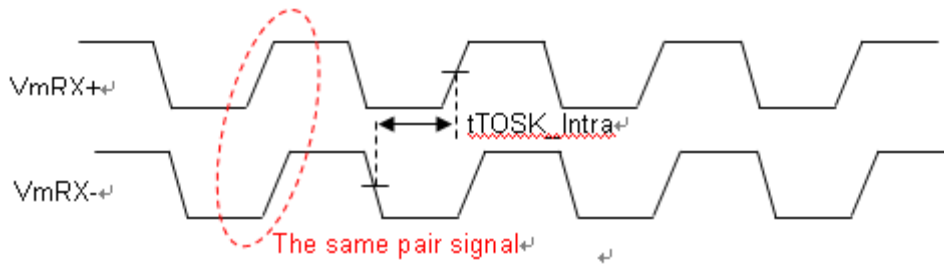
Note(2) Main Link Eye Diagram



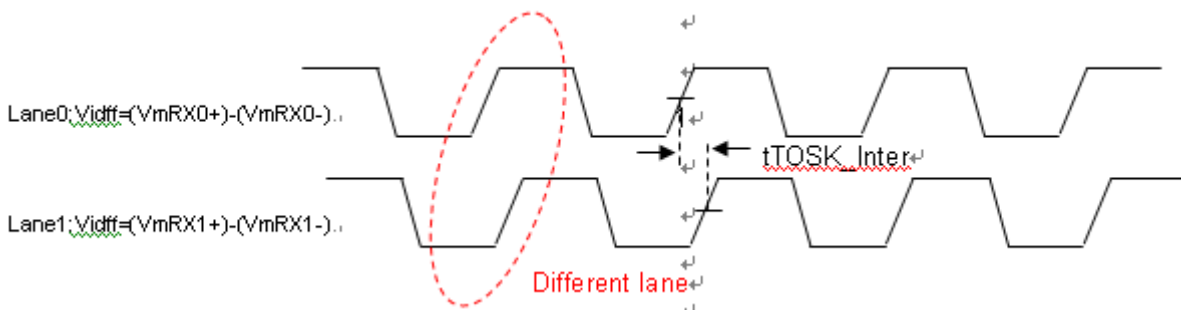
Point	High Bit Rate 2 @ TP3 EQ	
	Time(UI)	Voltage(V)
1	Any UI location (x) where the eye width is open from x to x+0.38UI	0.000
2	Any passing UI location between 0.375UI-0.625UI	0.045
3	Point 1 + 0.38UI	0.000
4	Same as Point 2	-0.045

[EYE Mask Vertices at embedded DP Sink Connector Pins]

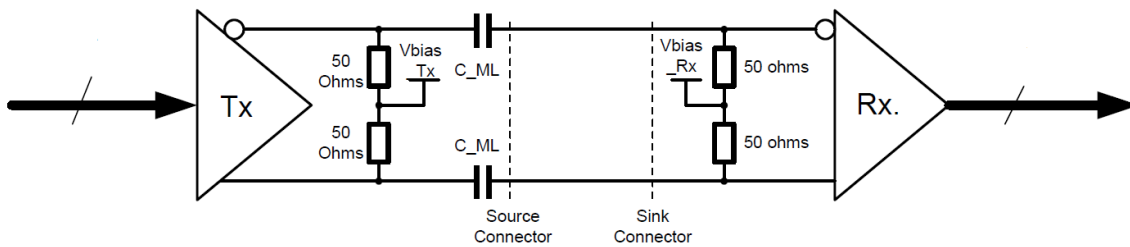
Note(3) eDP Intra-pair skew



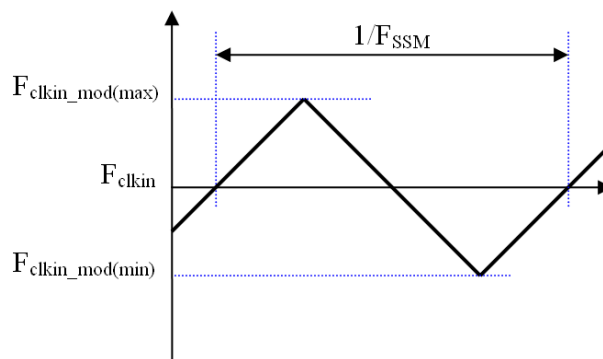
Note(4) eDP Inter-pair skew



Note(5) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_{ML_Source}) should be placed on the source device



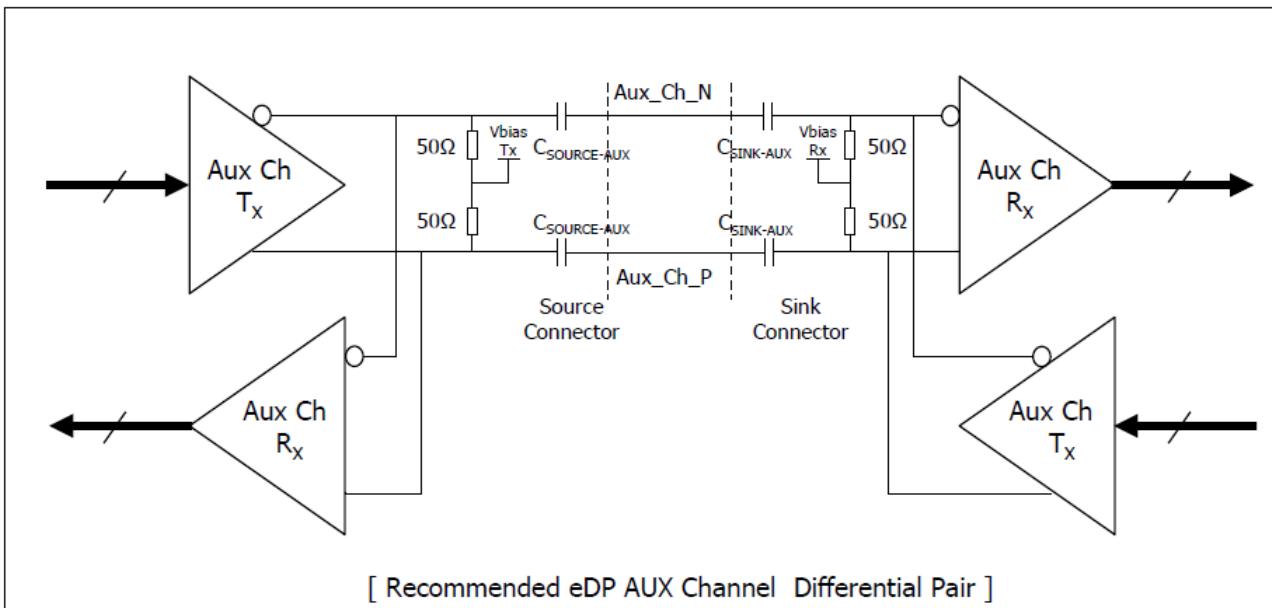
Note(6) The SSCG (Spread spectrum clock generator) is defined as below figures.



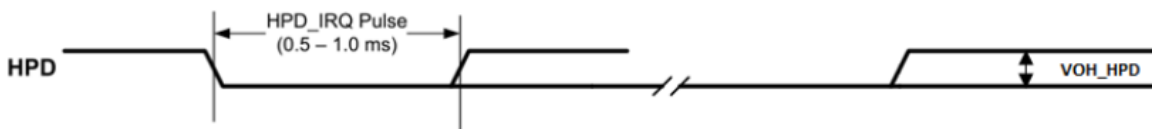
5.3.2 eDP AUX CHANNEL SIGNAL

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	us	
AUX Jitter at Tx IC Pins	T jitter	-	-	0.04	UI	
AUX Jitter at Rx IC Pins	T jitter	-	-	0.05	UI	
AUX Peak-to-peak voltage at Connector Rx Pins	VAUX-DIFFp-p	0.27	-	1.36	mV	
AUX Peak-to-peak voltage at Connector Tx Pins	VAUX-DIFFp-p	0.29	-	1.38	V	
AUX Differential termination resistance	AUX_dtr	80	100	120	ohm	
AUX DC common mode voltage	VAUX_CM	0	-	1.2	V	
AUX AC Coupling Capacitor	C_Source_Aux	75	-	200	nF	(1)

Notes(1) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Source_Aux) should be placed on the source device.



5.5.3 eDP HPD SIGNAL

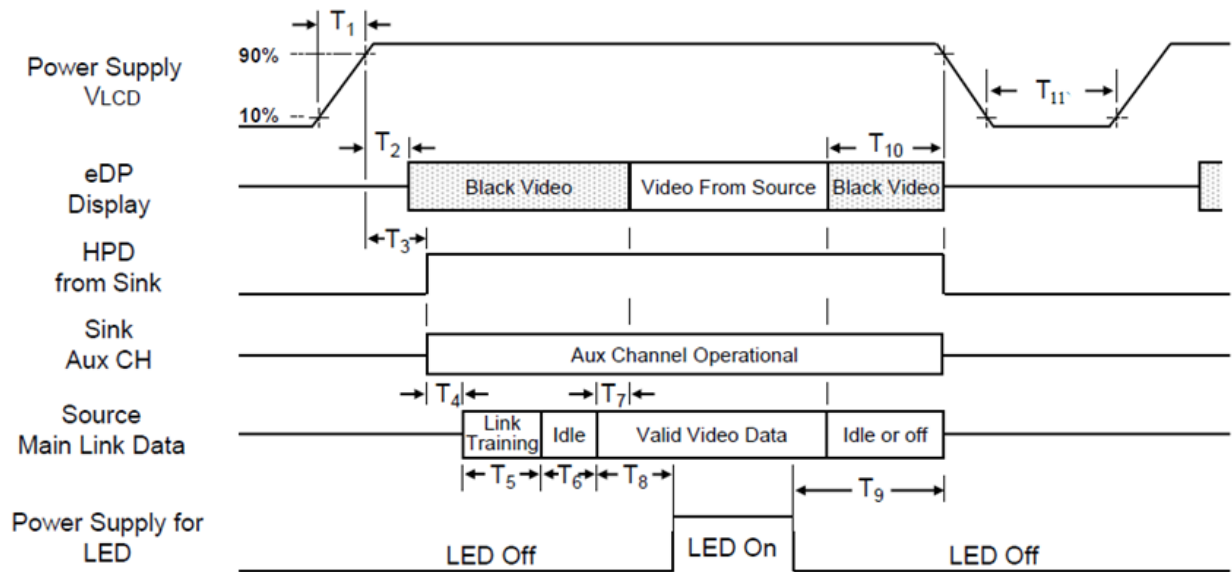


Parameter	Symbol	Min	Typ	Max	Unit
HPD Voltage	VOH_HPDP	3.135	-	3.465	V
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms

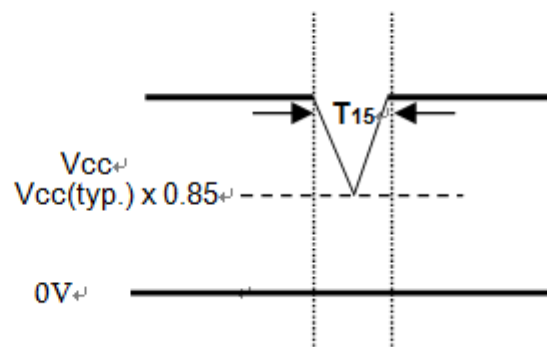
5.3.4 eDP RGB DATA MAPPING

Lane 0	Lane 1	Lane 2	Lane 3
R0-9:2	R1-9:2	R2-9:2	R3-9:2
R0-1:0 G0-9:4	R1-1:0 G1-9:4	R2-1:0 G2-9:4	R3-1:0 G3-9:4
G0-3:0 B0-9:6	G1-3:0 B1-9:6	G2-3:0 B2-9:6	G3-3:0 B3-9:6
B0-5:0 R4-9:8	B1-5:0 R5-9:8	B2-5:0 R6-9:8	B3-5:0 R7-9:8
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-9:2	G5-9:2	G6-9:2	G7-9:2
G4-1:0 B4-9:4	G5-1:0 B5-9:4	G6-1:0 B6-9:4	G7-1:0 B7-9:4
B4-3:0 R8-9:6	B5-3:0 R9-9:6	B6-3:0 R10-9:6	B7-3:0 R11-9:6
R8-5:0 G8-9:8	R9-5:0 G9-9:8	R10-5:0 G10-9:8	R11-5:0 G11-9:8
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-9:2	B9-9:2	B10-9:2	B11-9:2
B8-1:0 R12-9:4	B9-1:0 R13-9:4	B10-1:0 R14-9:4	B11-1:0 R15-9:4
R12-3:0 G12-9:6	R13-3:0 G13-9:6	R14-3:0 G14-9:6	R15-3:0 G15-9:6
G12-5:0 B12-9:8	G13-5:0 B13-9:8	G14-5:0 B14-9:8	G15-5:0 B15-9:8
B12-7:0	B13-7:0	B14-7:0	B15-7:0

5.4 POWER ON/OFF SEQUENCE



Vcc Dip[⊕]
T15 ≤ 10ms[⊕]



Timing	Required By	Min	Max	Units	Notes
T1	Source	0.5	10	ms	
T2	Sink	10	200	ms	
T3	Sink	15	200	ms	
T4	Source	0	-	ms	(7)
T5	Source	0	-	ms	(7)
T6	Source	0	100	ms	
T7	Sink	0	50	ms	
T8	Source	200	-	ms	
T9	Source	200	-	ms	(8)
T10	Source	0	500	ms	
T11	Source	1000	-	ms	

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen..

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance .

If $T2 < 0$, that maybe cause electrical overstress failure.

Note (4) T11 should be measured after the module has been fully discharged between power off and on period..

Note (5) Interface signal shall not be kept at high impedance when the power is on

Note (6) Vcc must decay smoothly when power-off

Note (7) Link training duration is dependent on the customer's system.

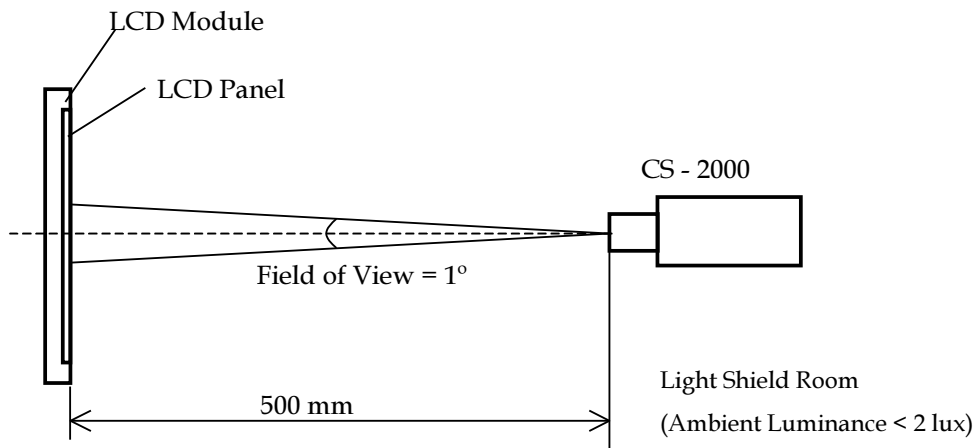
Note (8) LED power must be turned off while Video data signal is valid .

6. OPTICAL CHARACTERISTICS

6.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



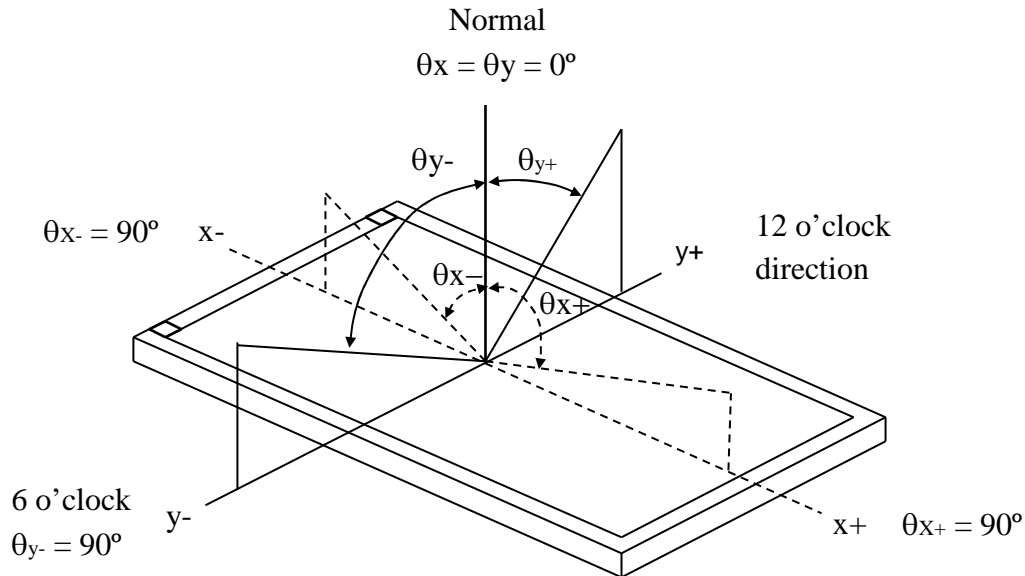
6.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 6.1. The following items should be measured under the test conditions described in 6.1 and stable environment shown in 6.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note					
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	700	1000	-	-	(2)					
Response Time		Gray to gray			14	20	ms	(3)					
Center Luminance of White		L _C		400	500	-	cd/m ²	(4)					
White Variation		δW				1.3	-	(6)					
Cross Talk		CT		-		4	%	(5)					
Color Chromaticity	Red	R _x		0.03	Typ.-	0.03	Typ.+	-					
		R _y						(0.674)		-			
	Green	G _x						(0.321)		-			
		G _y						(0.266)		-			
	Blue	B _x						(0.691)		-			
		B _y	(0.154)					-					
	White	W _x	(0.037)					-					
		W _y	0.306					-					
	Correlated color temperature							-		7000	-	K	
	Color Gamut		C.G.					-		95	-	%	DCI-P3
Viewing Angle	Horizontal	θ_{x+}	CR \geq 10	80	89	-	Deg.	(1)					
		θ_{x-}											
	Vertical	θ_{y+}											
		θ_{y-}											

Note (1) Definition of Viewing Angle (θ_x, θ_y) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

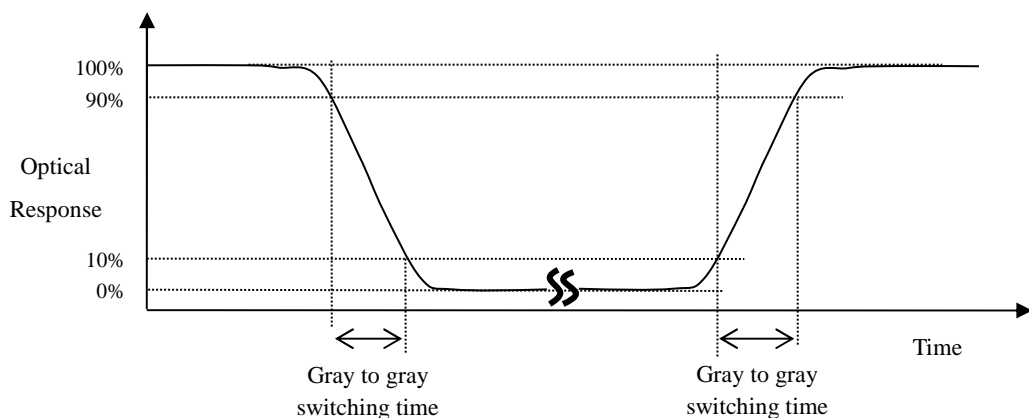
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (X), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}) :

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$, where $L(X)$ is corresponding to the luminance of the point X at the figure in Note (6).

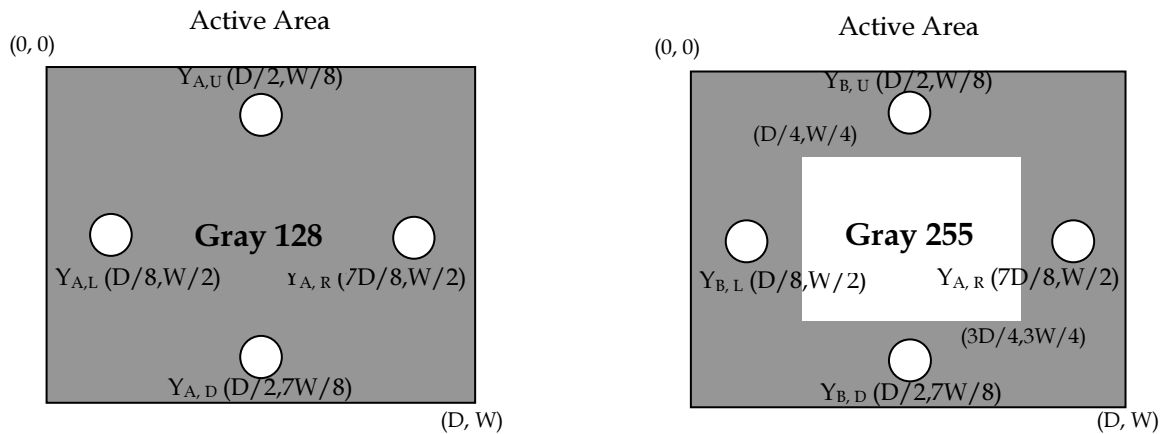
Note (5) Definition of Cross Talk (CT) :

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m²)

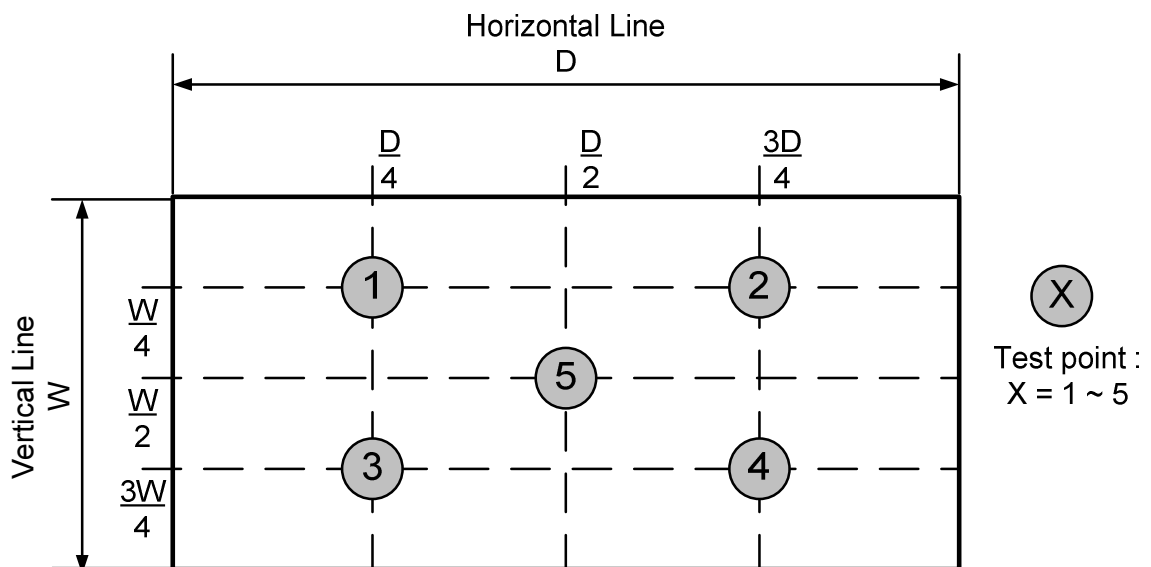
Y_B = Luminance of measured location with gray level 255 pattern (cd/m²)



Note (6) Definition of White Variation (δW) :

Measure the luminance of gray level 255 at 5 points

$$\delta W = \frac{\text{Maximum } [L(1), L(2), L(3), L(4), L(5)]}{\text{Minimum } [L(1), L(2), L(3), L(4), L(5)]}$$



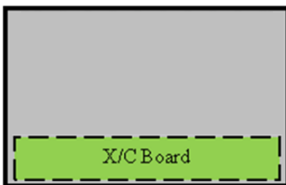
7. PRECAUTIONS

7.1 SAFETY PRECAUTIONS

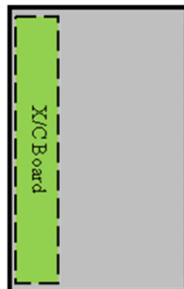
To optimize the lifetime and functions of PID SET, operating conditions should be followed as below

- [1] Normal operating condition
 - [1.1] Well-ventilated place is suggested to set up PID Set and system.
 - [1.2] Display pattern: regular switched patterns or moving pictures.
- [2] Operation usage to protect against image sticking due to long-term static display.
 - [2.1] Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static)display and 10 seconds' moving image.
 - [2.2] Periodical display contents should be changed from static image to moving picture.
 - [2.2.1] Different background and image colors changed respectively, and changed colors periodically.
 - [2.2.2] Background and image with large different luminance displayed at the same time should be avoided.
 - [2.2.3] Periodical power-off the system for a while or screen saver is needed after long-term static display.
 - [2.2.4] Moving picture or black pattern is strongly recommended for screen saver.
- [3] The startup voltage of a Backlight may cause an electrical shock while assembling with the converter.
Do not disassemble the module or insert anything into the Backlight unit.
- [4] Do not connect or disconnect the module in the "Power On" condition.
- [5] Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature...) Otherwise the module may be damaged.
- [6] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [7] Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, especially combining severe conditions such as high temperature/humidity, display stationary patterns, or long operation time etc..., it is strongly recommended to contact INX for field application engineering advice. Otherwise, the panel may be damaged and its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and full outdoor display.
- [8] LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.
- [9] Module should be turned clockwise (regular front view perspective) when used in portrait mode.

Landscape (Front view)



Portrait (Front view)



7.2 SAFETY STANDARDS

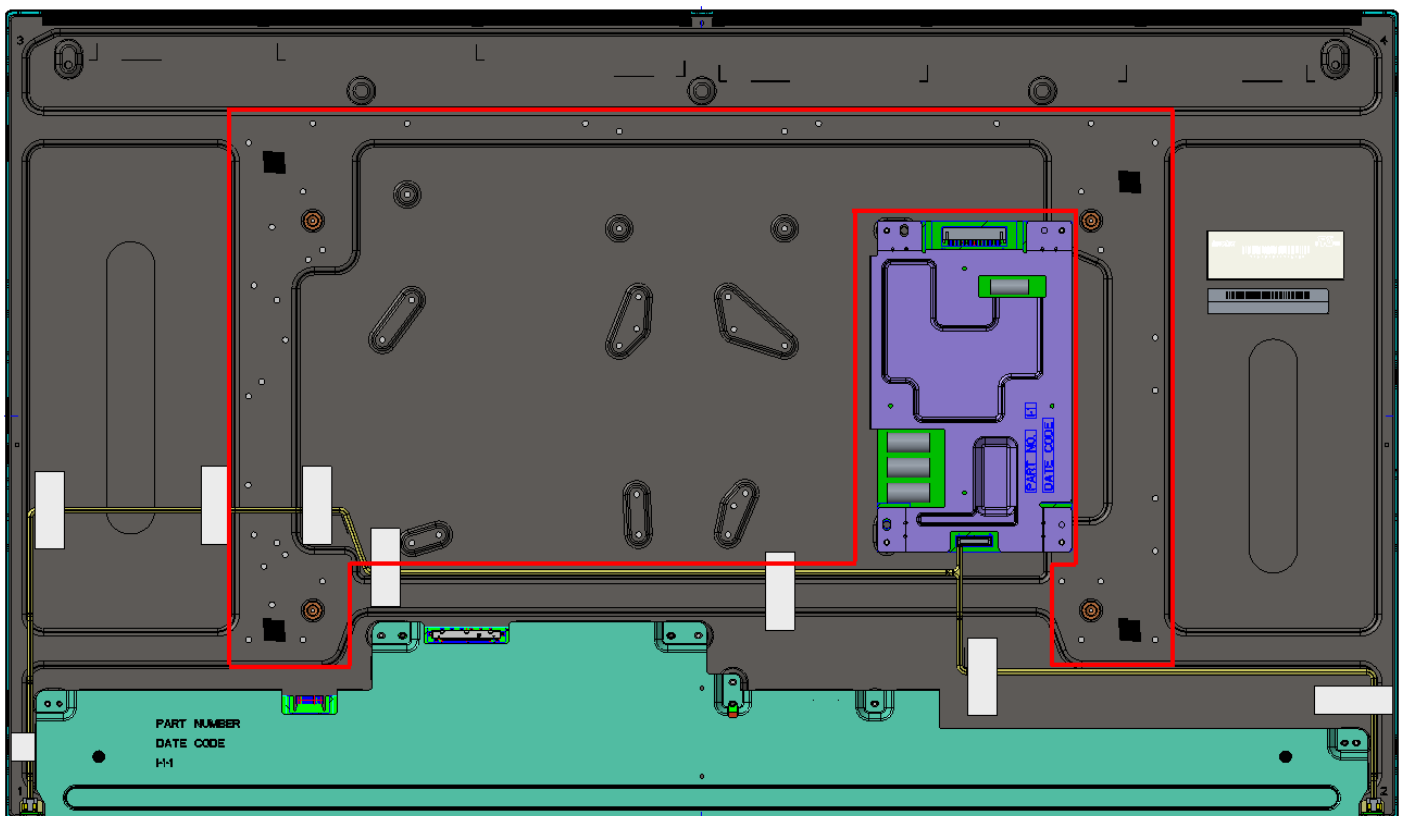
The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Audio/video, Information and Communication Technology Equipment	UL	UL 62368-1, 3rd Edition, 2021-10-22
	cUL	CAN/CSA C22.2 No. 62368-1:19, 3rd Edition, 2021-10-22
	CB	IEC 62368-1:2018 EN IEC 62368-1:2020+A11:2020

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

7.3 DUST RESIST

- [1] INX module dust test is conducted with marked holes (see figure below, marked with red box area) sealed.
- [2] Module users should design set with these holes used/sealed (if not used) or covered by set mechanism to prevent dust from entering. The INX testing procedure cannot replicate all different real world scenarios, module users should apply set dust resistance solution to meet user’s requirement.



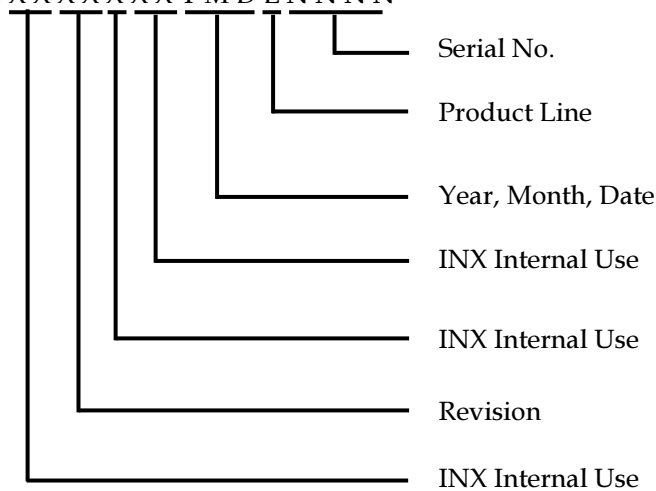
8. DEFINITION OF LABELS

8.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: S315DJ1-A01
- (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
- (c) Serial ID: XXXXXYYMDLNNNN

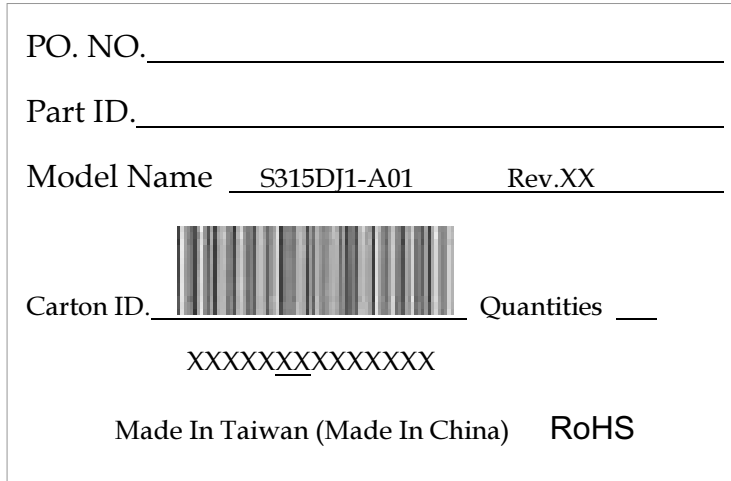


Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.
- (b) Revision Code: Cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 → Line1, 2 → Line 2, ...etc.

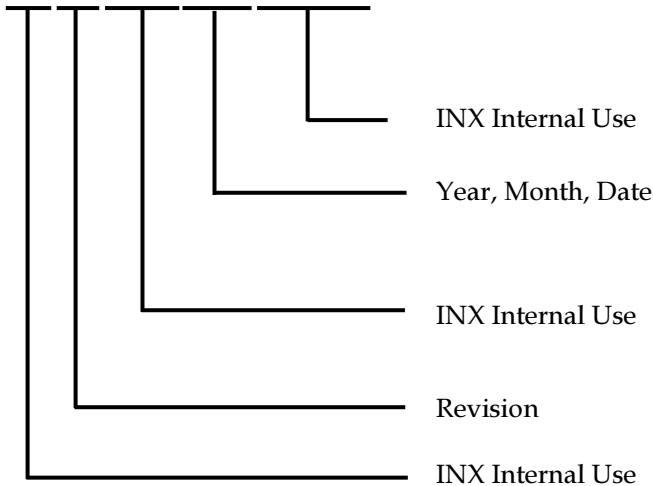
8.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.



Model Name: S315DJ1-A01

Carton ID: X X X X X X Y M D X X X X



Serial ID includes the information as below :

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2...etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code: Cover all the change

9. PACKAGING

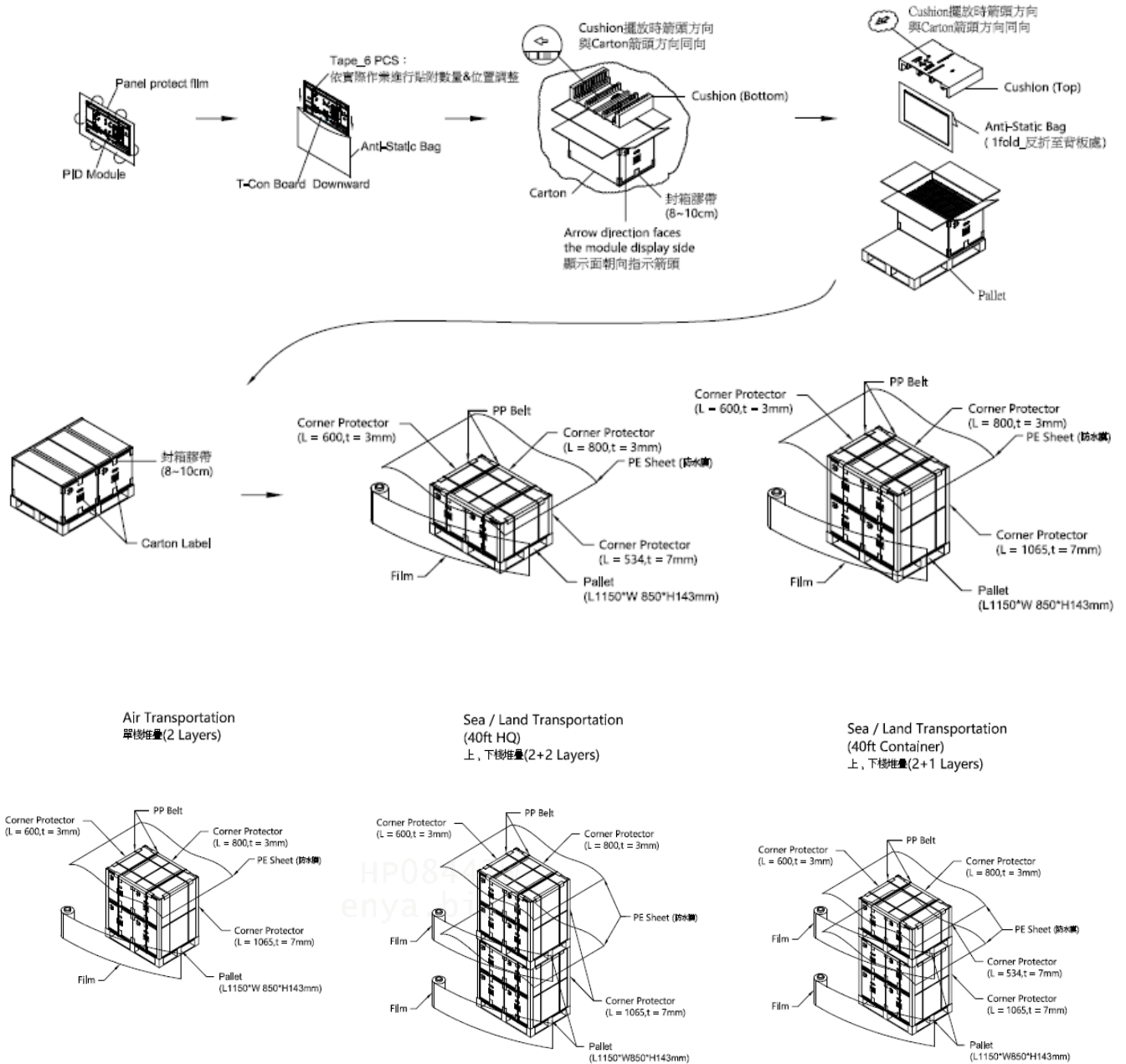
9.1 PACKAGING SPECIFICATIONS

- (1) 12 LCD PID modules / 1 Box
- (2) Box dimensions : 830(L) X 565 (W) X 531 (H)
- (3) Weight: approximately 45 Kg (12 modules per box)

9.2 PACKAGING METHOD

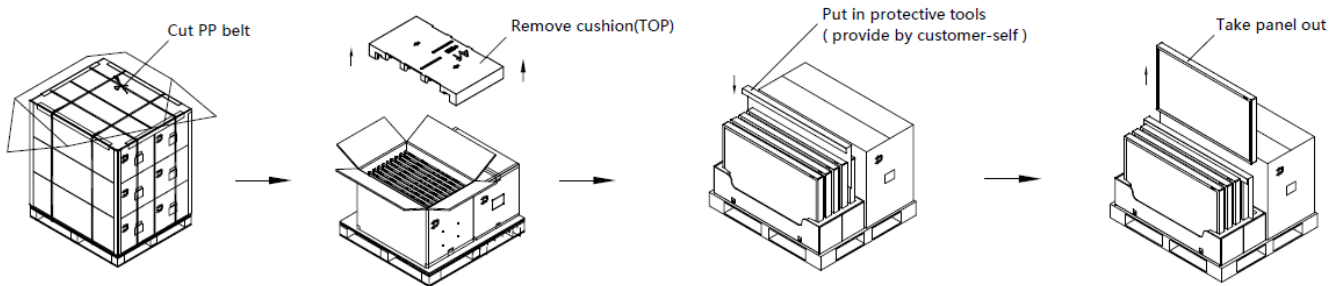
Packaging method is shown in following figures

Packing (1) Carton dimensions: 830(L)x565(W)x531(H)mm
(2) 12 PID Mod / Carton



9.3 UN-PACKAGING METHOD

Un-packaging method is shown as following figures.



10. MECHANICAL CHARACTERISTIC

