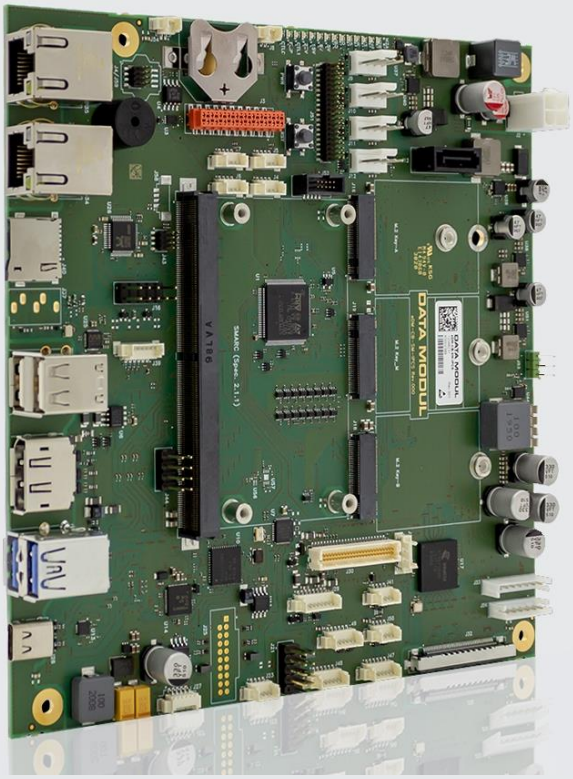
DATA MODUL

eDM-CB-SM-IPCS



Document Revision History

Revision	Revision History	Date
00	Draft version	12.12.2021

Reference to this Operating Manual

The purpose of all the figures and illustrations in this User Manual is merely to provide a better explanation and can differ to the actual appearance of the devices. They are to be understood as schematic representations.

© 2021 DATA MODUL AG. All rights reserved.

Trademarks:
Although all the information contained within this document is carefully checked, no guarantee of correctness is implied or expressed. All brand or product names are trademarks or registered trademarks of their respective owners.
Technical and optical changes as well as misprints reserved.

Contents

1. Preface

1.1. Using this Document

- In this Document, the eDM-CB-SM-IPCS is also referred to as „CB“.
- Please read this Document before using this Carrier Board (CB).
- This Document contains information about the hardware, software and configuration of the eDM-CB-SM-IPCS.
- Awareness of the safety instructions and instructions for use in this Document will ensure the safe and correct use of the eDM-CB-SM-IPCS.
- In addition to the information given here, you should comply with the local regulations for the prevention of accidents and generally applicable safety regulations.

1.2. Purpose of this Document

The purpose of this document is the definition of the technical parameters, the electrical connections and the mechanical dimensions of the eDM-CB-SM-IPCS.

1.3. Danger Symbols & Levels

In this Document, symbols are used to highlight important safety instructions and any advice relating to the board. The instructions should be followed very carefully to avoid any risk of accident, personal injury or property damage.

Danger Symbols

	Dangerous Voltage, danger of electric shock
	Hazard point
	All DATA MODUL AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a DATA MODUL AG product except at an electrostatic-free workstation. Additionally, do not ship or store DATA MODUL AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the DATA MODUL AG Limited Warranty.

Danger Levels

DANGER	Indicates a hazardous situation, which will result in death or serious injury.
WARNING	Indicates a hazardous situation, which could result in death or serious injury.
CAUTION	Indicates a hazardous situation, which may result in minor or moderate injury.
NOTICE	Indicates a property damage.

General Symbols

	Additional support or useful information.
	The crossed-out refuse bin indicates that the products have to be properly recycled or disposed of in accordance with national legislation in the respective EU countries. If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the local regulations.

1.4. Technical Support

DATA MODUL's technicians and engineers are committed to provide the best possible technical support for our customers to enable an easy use and implementation of our products. We recommend to visit our website at www.data-modul.com first for the latest documentation, utilities and drivers, which have been made available to assist you. If you need further assistance after visiting our website please contact our technical support department by email at support@data-modul.com.

1.5. List of Abbreviations

Abbreviation	Description
BOM	Bill of Materials
CB	Carrier Board
CMOS	Complementary MOS
CSI	MIPI-Camera Serial Interface
DFP	Downstream Facing Port (USB Type-C)
DMIS	Data Modul Inhouse Stanard
DP	DisplayPort or Differential Pair in relation to Pin Type
DSI	MIPI-Display Serial Interface
EMI	Electro Magnetic Interference
EN	European Norm
FFC	Flat Foil Cable
FHD	Full-HD Graphics Resolution
GBE	Gigabit Ethernet
GND	Ground
GPIO	General purpose Input/Output
HDA	High Definition Audio Interface
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit Bus
I2S-Audio	I2S Audio Interface
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LVDS	Low-Voltage Differential Signaling
NA	Not Available
NC	Not Connected
PCB	Printed Circuit Board
PCIe	PCI Express
PMC	Management Controller
PWM	Pulse Width Modulation
RefDes	Reference Designator
RTC	Real Time Clock
SATA	Serial ATA
SMBus	System Management Bus
SPI	Serial Peripheral Interface
TBD	To Be Defined
TMDS	Transition-Minimized Differential Signaling.
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
Vx1	V-By-One Display Interface

1.6. General Connector Signal Description

Type	Description
IO	Bi-directional
I	Input
O	Output
GND	Ground connection
Power	Power connection
NC	Not connected
Analog	Analog signal
DP	Differential pair

1.7. Industry Specifications

Specification	Link
SMARC Hardware Specification 2.1.1	http://sget.org
Extended Display Identification Data Standard EDID™	http://www.vesa.org
Enhanced Display Data Channel Specification DDC	http://www.vesa.org
Universal Serial Bus (USB) Specification	http://www.usb.org/home
Serial ATA Specification	http://www.serialata.org
High Definition Audio Specification	http://www.intel.com
IEEE standard 802.3ab 1000BASE-T Ethernet	http://www.ieee.org

2. Standards & Certifications

2.1. SMARC Standard

eDM-CB-SM-IPCS is compliant to SMARC 2.0 and SMARC 2.1.1 specification.

2.2. Material Compliance

The PCB is produced under lead free soldering conditions.
All components are produced according to European RoHS (RoHS-1 = 2002/95/EU, RoHS-2 = 2011/65/EU) and REACH (2006/1907/EU) regulations.

2.3. EMC Standards

Design to meet EN 55032-B within enclosure
EN61000-4-2 contact discharge 4kV
EN61000-4-2 air discharge 8kV

2.4. Safety

Designed to meet EN60950, EN62638 and UL60950.

2.5. Shock & Vibration

Designed to meet IEC/EN60068 and IEC/EN60068-2-27

2.6. Environmental Conditions

The eDM-CB-SM-IPCS is able to be operated and stored under the following environmental conditions:

- Temperature (operating): 0°C … +60°C (commercial grade)
- Temperature (storage): -15°C … +60°C
- Relative humidity: < 90%

2.7. Functional Block Diagram

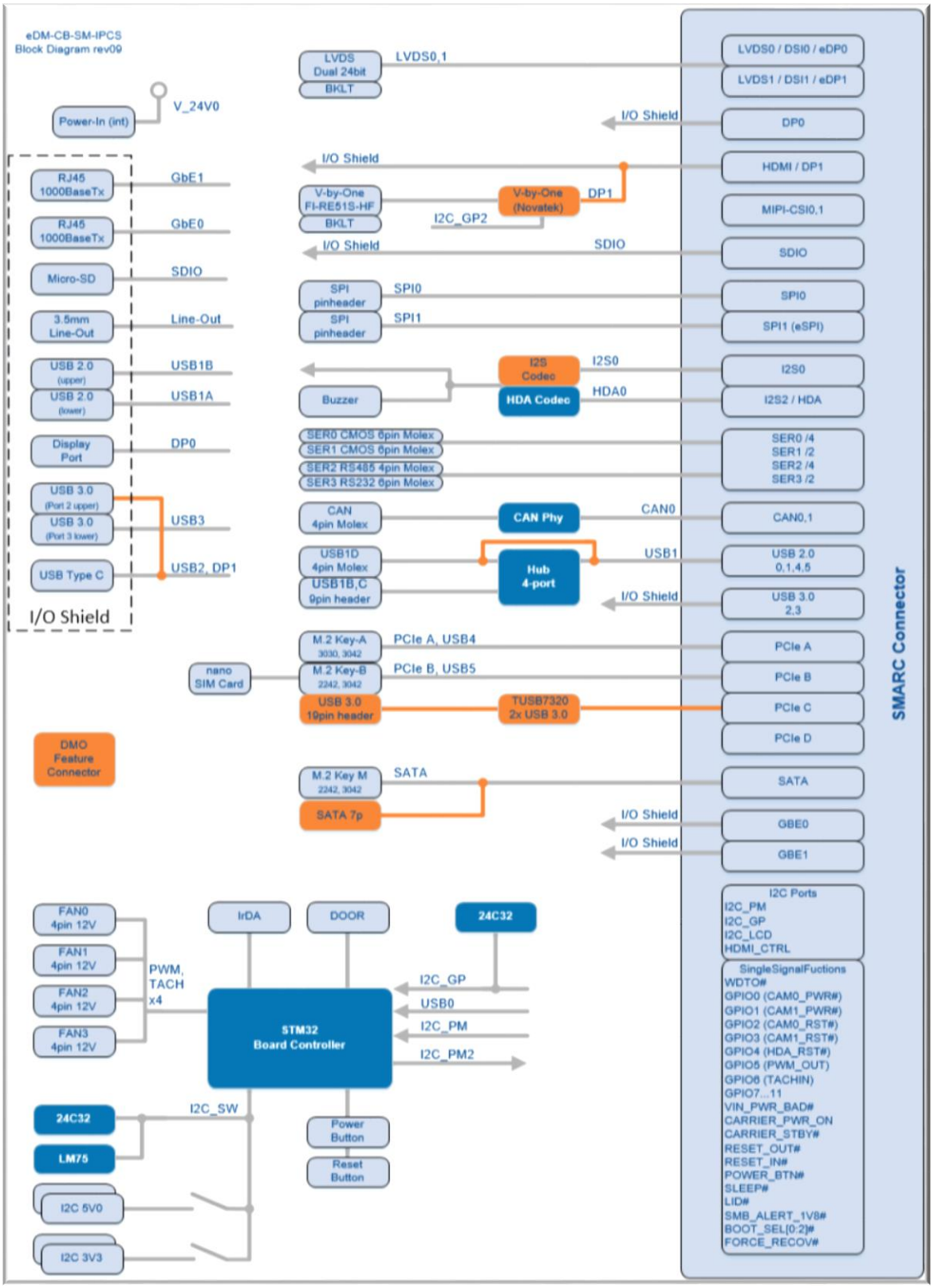


Figure 1 Functional Block Diagram

2.8. Ordering Information

Model Name	Part No.	Description
eDM-CB-SM-IPCS	12048231	SMARC 2.1.1 Carrier Board with full sampled parts according to the Data Modul HW Specification for this product.

2.9. Connector Positions

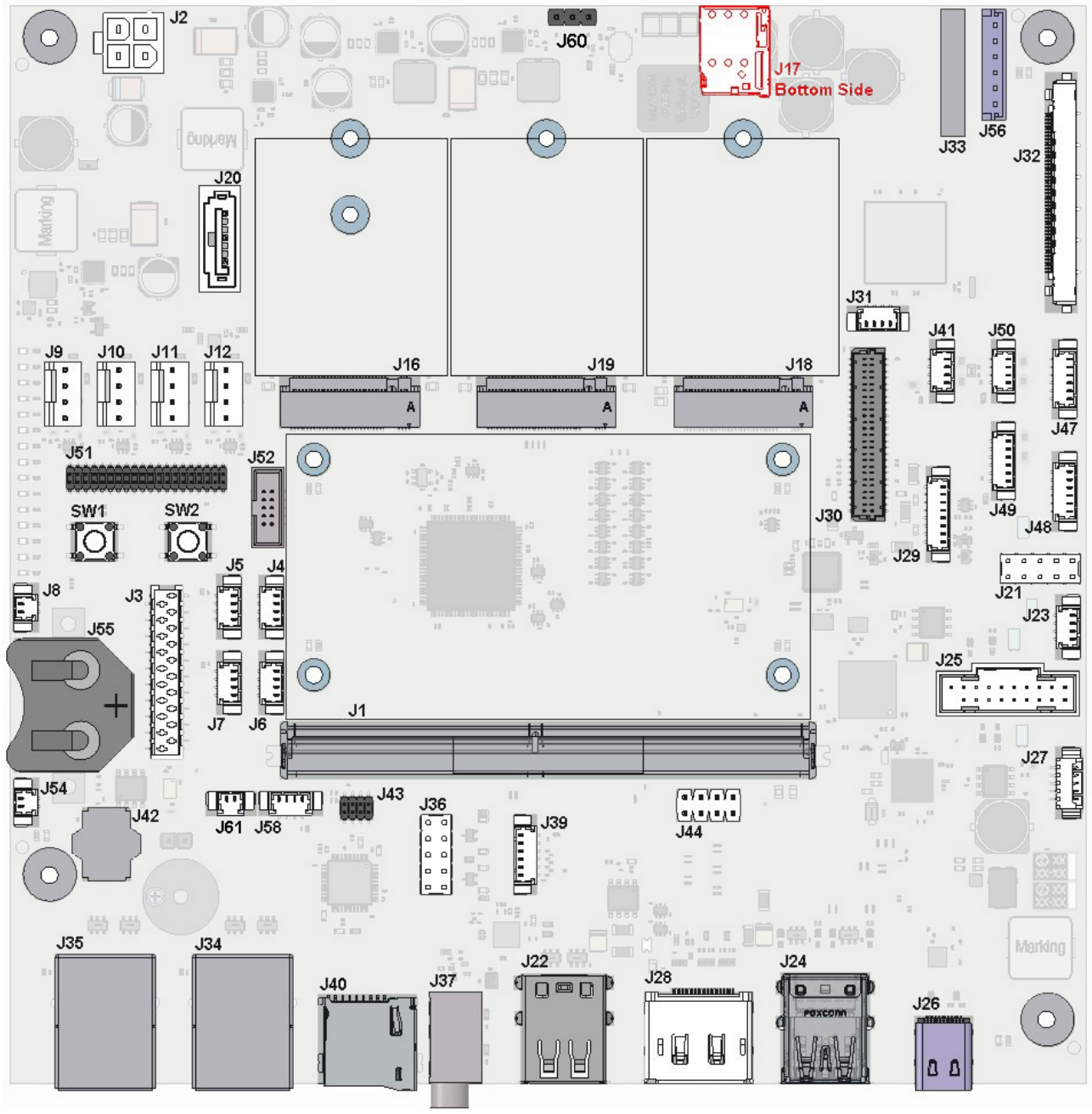


Figure 2 Connector Positions

2.10. Connector List

Reference Designator	Interface / Function
J1	SMARC module connector
J2	Power In Connector (24V)
J3	Data Modul IR-keyboard interface connector
J4	I2C_SW interface connector from STM32 board controller (CMOS-5V)
J5	I2C_SW interface connector from STM32 board controller (CMOS-5V)
J6	I2C_SW interface connector from STM32 board controller (CMOS-3.3V)
J7	I2C_SW interface connector from STM32 board controller (CMOS-3.3V)
J8	Door contact connector
J9	System FAN1 connector
J10	System FAN2 connector
J11	System FAN3 connector
J12	System FAN4 connector
J16	M.2 Key-A connector
J17	SIM-Card socket (only in combination with J18)
J18	M.2 Key-B connector
J19	M.2 Key-M connector
J20	SATA L-Shape connector
J21	USB2.0 (9-pin) internal pin-header
J22	USB2.0 dual Type-A connector on IO-shield
J23	USB 2.0 Port (1D) Molex-PicoBlade internal connector
J24	USB3.0 Dual Type-A connector on IO-shield
J25	USB3.0 (19-pin) internal pin-header
J26	USB single Type-C
J27	USB Type-C SPI-programming connector (internal use only)
J28	DisplayPort connector on IO-shield (DDI0 from SMARC)
J29	Backlight connector for LVDS display
J30	LVDS Display connector
J31	V-By-One Debug Connector (internal use only)
J32	V-By-One Display connector
J33	Backlight connector for V-By-One display
J34	Gigabit ethernet-0 connector
J35	Gigabit ethernet-1 connector
J36	Audio frontpanel pin-header
J37	Audio line-out connector
J39	I2S audio microphone connector

J40	Micro-SD card socket
J41	CAN-bus connector
J42	SPI0 pin-header
J43	SPI1 pin-header
J44	Boot-select jumpers
J47	UART 1.8V connector (SER0)
J48	UART 1.8V connector (SER1)
J49	RS232 connector (SER3)
J50	RS485 connector (SER2)
J51	Data Modul feature connector (Rev.100)
J52	FW-update/debug for STM32-board controller (internal use only)
J54	RTC-battery internal connector
J55	RTC battery CR2032 socket
J56	Optional TCON voltage connector for V-By-One display
J58	GbE0/1 PTP (Precision Time Protocol) extension
J60	V-By-One TCON voltage selection jumper
J61	Power button internal connector
SW1	Power button
SW2	Reset button

2.11. Power Supply

Input Voltage

- VCC: 24.0 V ± 5%
- Voltage Ripple: max. 100mV peak to peak 0 … 20 MHz
- Rise Time: 0.1 … 20ms from input voltage < 10% nominal VCC
- Max. inrush current VCC: 5A
- Max. supply current 12A.
- The maximum supply current must be limited to 12A by the power supply unit!

3. External Connectors (IO-Shield)

3.1. Gigabit Ethernet 0/1

Reference designator: – J34(GBR0) / J35(GBE1)

Description

The eDM-CB-SM-IPCS provides two gigabit ethernet ports of the SMARC module GBE0 on J34 and GBE1 on J35. Each of RJ-45 connectors has integrated magnetics and two LEDs for link activity and mode indication.

Interfaces used

Media depended interface (MDI) 0 of the SMARC module on J34
Media depended interface (MDI) 1 of the SMARC module on J35

Connector drawing and contact-numbering scheme

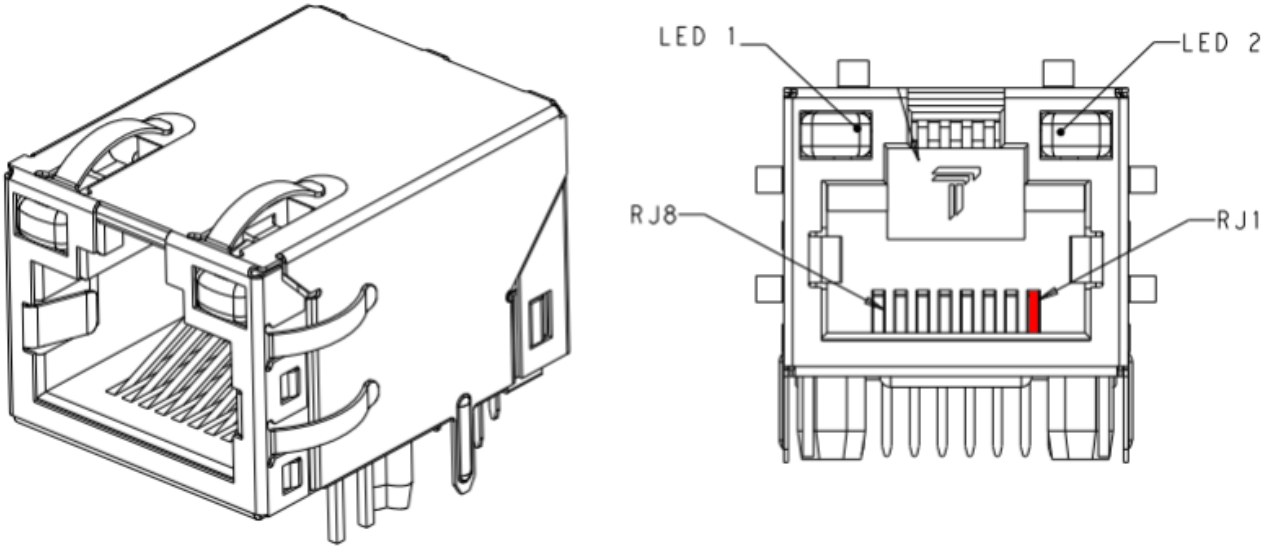


Figure 3 Connector – J34/J35

LED Indication

Mode	LED 1	LED 2
Link		yellow
1000Mbit	orange	yellow blinking
100Mb	green	yellow blinking
10Mb	off	yellow blinking

3.2. Micro-SD Socket

Reference designator: J40

Micro-SD connector; ultra-low-profile; push-push type

Description

The micro-SD ultra-low-profile, push-push type socket provides 4-bit SDIO interface of the SMARC module. The SDIO performance is depended on used SMARC module platform.

Interfaces used

SDIO interface of the SMARC module

Connector drawing and contact-numbering scheme

Figure 4 Micro-SD Socket – J40

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J40	1	SDIO_DATA2	IO (1.8/3.3V)	Serial data line 2
	2	SDIO_DATA3	IO (1.8/3.3V)	Serial data line 3
	3	SDIO_CMD	IO (1.8/3.3V)	Command Line
	4	VCC	Power(3.3V)	3.3V power-supply for connected device; max. current 100mA
	5	SDIO_CLK	O (1.8/3.3V)	Data clock
	6	GND	GND	Device power ground
	7	SDIO_DATA0	IO (1.8/3.3V)	Serial data line 0
	8	SDIO_DATA1	IO (1.8/3.3V)	Serial data line 1

3.3. Line-Out Audio Connector

Reference Designator: – J37

Green 3,5mm stereo-audio jack with presence detect support.

Description

This connector provides audio line-out optional either of the HD-Audio codec (ALC888S) or I2S codec (WM8904).
See more details about shard resources in chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

Line-out signals of the HDA or I2S audio codec

Connector drawing and contact-numbering scheme

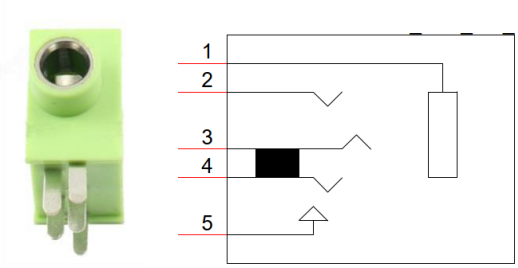


Figure 5 Connector – J37

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J37	1	GND	GND	Connected to ground potential of the PCB
	2	Line-Out left	O (Analog)	Audio line out (left channel)
	3	Line-Out right	O (Analog)	Audio line out (right channel)
	4	Presence detect in	I (Analog)	This input is connected to HDA codec resistor network
	5	GND	GND	Connected to ground potential of the PCB

3.4. USB 2.0 Dual Type-A Connector

Reference Designator: – J22

Description

Standard USB 2.0 Dual Type-A connector with supported cable length of max. 1,5 m.
Shared Port: USB Port 1B (upper port) is shared with the internal USB pin-header J21. Availability of one or the other interface dependent on exact product variant based on this electronic design.
For manual modifications of the Port routing, see Chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

USB 2.0 port 1B (upper connector port) of the USB hub)
USB 2.0 port 1A (upper connector port) of the USB hub)
Supplied by 5.0 V S5 voltage
Current limited to 500 mA for each port.

Connector drawing and contact-numbering scheme

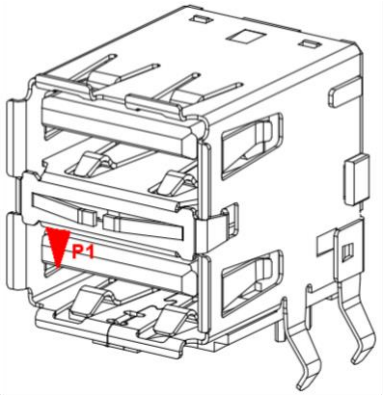


Figure 6 Connector – J22

Pinout

According to USB 2.0 Specification

3.5. DisplayPort Connector

Reference Designator: – J28

Description

One standard DisplayPort connector is provided on the front of the eDM-CB-SM-IPCS.

Interface used

DisplayPort DP0 from the SMARC module. The graphic performance is depended on used SMARC module.

Connector drawing and contact-numbering scheme

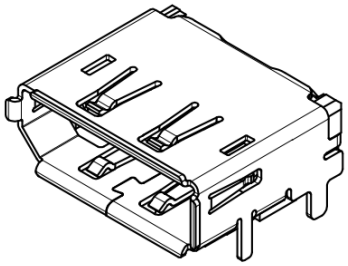


Figure 7 Connector – J28

3.6. USB 3.0 Dual Type-A Connector

Reference Designator: – J24

Description

Standard USB 3.0 Dual Type-A connector with supported cable length of max. 1,5 m.
Shared Port: USB 2.0 and 3.0 Port 2 (upper port) is shared with the USB Type-C connector J26.
Availability of one or the other interface dependent on exact product variant based on this electronic design.
For manual modifications of the Port routing, see Chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

USB 3.0 port 2 (shared port) and 3 for the SMARC module
USB 2.0 port 2 (shared port) and 3 of the SMARC module
Supplied by 5.0 V S5 voltage
Current limited to 900 mA for each port.

Connector drawing and contact-numbering scheme

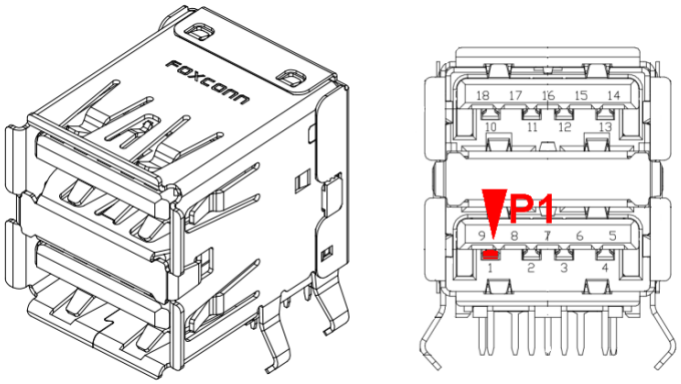


Figure 8 Connector – J24

3.7. USB Single Type-C Connector

Reference Designator: – J26

Description

The Carrier Board provides one single USB Type-C connector right-angled SMT/THT combined mounting.

Features supported

DisplayPort DP1 from the SMARC module (shared with V-By-One Transmitter)
USB 2.0 Port 2 from the SMARC module (shared with upper port of dual Type-A connector J24)
USB 3.2 (5.0 Gbit/s) Port 2 from the SMARC module (shared with upper port of dual Type-A connector J24)
See more details about shard resources in chapter **"Functional Exclusives and Shared Resources"**.

Power delivery PD3 (USB_PD_R3_0)

5,0V max. current: 3,0 A
9,0V max. current: 3,0 A
15,0V max. current: 3,0 A
20,0V max. current: 5,0 A

Connector drawing and contact-numbering scheme

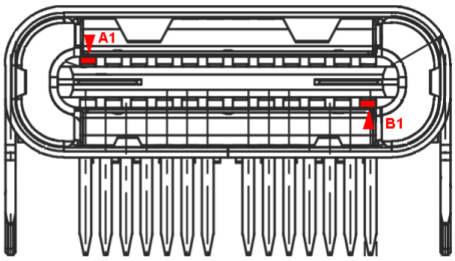


Figure 9 Connector – J26

4. Internal Connectors

4.1. SMARC Connector

Reference Designator: J1

Description

Socket and mechanical space including mounting holes and standoffs to support SMARC 2.0 / 2.1 modules according to the standards specification Rev. 2.1.1

Interfaces provided (excluding unused interfaces)

PCI Express Ports A,B,C
USB 2.0 Ports 0,1,4,5
USB 3.0 Ports 2,3
GBE 0, 1
SATA
LVDS 0,1
DisplayPort 0
DisplayPort 1
SDIO
SPI0
eSPI as SPI1 (SPI Mode)
I2S0, HDA
SER 0, 1, 2, 3
CAN 0
I2C_GP
I2C_PM
12 GPIOs
Power- and System-Status signalling

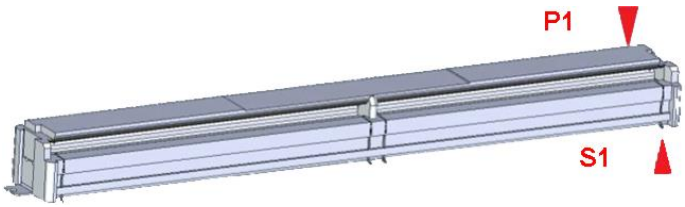


Figure 10 SMARC Connector – J1

Pinout (for more details about pinout , see to SMARC Specification 2.1.1)
Note: the input/output pin type/direction is described from the carrier board view.

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
P1	SMB_ALERT#	O (OD 1.8V-5V)	SMBus Alert# (Interrupt) signal	J44 Feature Connector and Board Controller STM32
P2	GND	GND	Connected to ground potential of the PCB	GND
P3	CSI1_CK+	O DP D-PHY	CSI1 differential clock input (point to point)	not connected on CB
P4	CSI1_CK-			
P5	GBE1_SDP	IO (CMOS 3.3V)	IEEE 1588 trigger signals (GBE[0]_SDP)	J58 (PicoBlade)
P6	GBE0_SDP	IO (CMOS 3.3V)	IEEE 1588 trigger signals (GBE[0]_SDP)	J58 (PicoBlade)

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
P7	CSI1_RX0+	O DP D/M-PHY	CSI1 differential input (point to point)	not connected on CB
P8	CSI1_RX0-			
P9	GND	GND	Connected to ground potential of the PCB	GND
P10	CSI1_RX1+	O DP D/M-PHY	CSI1 differential input (point to point)	not connected on CB
P11	CSI1_RX1-			
P12	GND	GND	Connected to ground potential of the PCB	GND
P13	CSI1_RX2+	O DP D/M-PHY	CSI1 differential input (point to point)	not connected on CB
P14	CSI1_RX2-			
P15	GND	GND	Connected to ground potential of the PCB	GND
P16	CSI1_RX3+	O DP D/M-PHY	CSI1 differential input (point to point)	not connected on CB
P17	CSI1_RX3-			
P18	GND	GND	Connected to ground potential of the PCB	GND
P19	GBE0_MDI3-	IO (GBE MDI)	Differential pair signals for external transformer	J34 (RJ45)
P20	GBE0_MDI3+			
P21	GBE0_LINK100#	I OD (CMOS 3.3V)	Link speed indication LED for GBE0 100Mbps	J34 (RJ45)
P22	GBE0_LINK1000#	I OD (CMOS 3.3V)	Link speed indication LED for GBE0 1000Mbps	J34 (RJ45)
P23	GBE0_MDI2-	IO (GBE MDI)	Differential pair signals for external transformer	J34 (RJ45)
P24	GBE0_MDI2+			
P25	GBE0_LINK_ACT#	I OD (CMOS 3.3V)	Link / activity indication for GBE0	J34 (RJ45)
P26	GBE0_MDI1-	IO (GBE MDI)	Differential pair signals for external transformer	J34 (RJ45)
P27	GBE0_MDI1+			
P28	GBE0_CTREF	Analog (0 to 3.3V)	Center-Tap ref. voltage for GBE0 magnetic	J34 (RJ45)
P29	GBE0_MDI0-	IO (GBE MDI)	Differential pair signals for external transformer	J34 (RJ45)
P30	GBE0_MDI0+			
P31	SPI0_CS1#	I (CMOS 1.8V)	SPI chip select 0 (SPI boot)	not connected on CB
P32	GND	GND	Connected to ground potential of the PCB	GND
P33	SDIO_WP	O OD (CMOS 1.8V/3.3V)	SDIO write protect	Tied to GND
P34	SDIO_CMD	IO (CMOS 1.8V/3.3V)	SDIO command/response	J40 (10R serial resistor)
P35	SDIO_CD#	IO (OD 1.8V/3.3V)	SDIO card detection	J40
P36	SDIO_CK	I (CMOS 1.8/3.3V)	SDIO clock	J40
P37	SDIO_PWR_EN	I (CMOS 3.3V)	SDIO power enable	Power Switch of Micro-SD Card
P38	GND	GND	Connected to ground potential of the PCB	GND
P39	SDIO_D0	IO (CMOS 1.8V/3.3V)	SDIO data lines. These signals operate in push-pull mode.	J40 (10R serial resistors)
P40	SDIO_D1			
P41	SDIO_D2			
P42	SDIO_D3			

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
P43	SPI0_CS0#	I (CMOS 1.8V)	SPI0 (Boot) chip select 0	J42
P44	SPI0_CK	I (CMOS 1.8V)	SPI0 (Boot) clock	J42
P45	SPI0_DIN	O (CMOS 1.8V)	SPI0 (Boot) MISO	J42
P46	SPI0_DO	I (CMOS 1.8V)	SPI0 (Boot) MOSI	J42
P47	GND	GND	Connected to ground potential of the PCB	GND
P48	SATA_TX+	I DP (LVDS)	Serial ATA channel 0 Transmit output differential pair	J19 or J20
P49	SATA_TX-			
P50	GND	GND	Connected to ground potential of the PCB	GND
P51	SATA_RX+	O DP (LVDS)	Serial ATA Channel 0 Reive Input Differential Pair	J19 or J20
P52	SATA_RX-			
P53	GND	GND	Connected to ground potential of the PCB	GND
P54	SPI1_CS0#	I (CMOS 1.8V)	SPI1 chip select 0	J43
P55	SPI1_CS1#	I (CMOS 1.8V)	SPI1 chip select 1	not connected on CB
P56	SPI1_CK	I (CMOS 1.8V)	SPI1 clock	J43
P57	SPI1_DIN	O (CMOS 1.8V)	SPI1 MISO	J43
P58	SPI1_DO	I (CMOS 1.8V)	SPI1 MOSI	J43
P59	GND	GND	Connected to ground potential of the PCB	GND
P60	USB0+	IO DP	USB differential data pairs for port 0	Board Controller STM32
P61	USB0-			
P62	USB0_EN_OC#	IO OD (3.3V)	USB over-current sense and power enable port 0	not connected on CB
P63	USB0_VBUS_DET	O (USB VBUS 5V)	USB Port 0 host power detection	not connected on CB
P64	USB0_OTG_ID	O OD	USB OTG Indication to Hot	not connected on CB
P65	USB1+	IO DP	USB differential data pairs for port 1	USB2.0 Hub or J23
P66	USB1-			
P67	USB1_EN_OC#	IO OD (3.3V)	USB over-current sense and power enable port 1	not connected on CB
P68	GND	GND	Connected to ground potential of the PCB	GND
P69	USB2+	IO DP	USB differential data pairs for port 2	USB Type-C or J23(USB3.0 upper port)
P70	USB2-			
P71	USB2_EN_OC#	IO OD (3.3V)	USB over-current sense / power enable port 2	USB Power Supervisor
P72	RSVD	-	NC	not connected on CB
P73	RSVD	-	NC	not connected on CB
P74	USB3_EN_OC#	IO OD (3.3V)	USB over-current sense / power enable port 3	USB Power Supervisor
	Key			
P75	PCIE_A_RST#	I (CMOS 3.3V)	PCIe port A reset output from module	J16 (M.2 Key-A)
P76	USB4_EN_OC#			
P77	PCIE_B_CKREQ#	O OD (CMOS 3.3V)	PCIe port B clock request	J18
P78	PCIE_A_CKREQ#	O OD (CMOS 3.3V)	PCIe port A clock request	J16 (M.2 Key-A)

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
P79	GND	GND	Connected to ground potential of the PCB	GND
P80	PCIE_C_REFCK+	I DP (PCIE)	Differential PCIe link C reference	USB3.0 Controller
P81	PCIE_C_REFCK-		clock input	
P82	GND	GND	Connected to ground potential of the PCB	GND
P83	PCIE_A_REFCK+	I DP (PCIE)	Differential PCIe link A reference	J16 (M.2 Key-A)
P84	PCIE_A_REFCK-		clock input	
P85	GND	GND	Connected to ground potential of the PCB	GND
P86	PCIE_A_RX+	O DP (PCIE)	Differential PCIe link A receive data pair	J16 (M.2 Key-A)
P87	PCIE_A_RX-			100nF AC coupled
P88	GND	GND	Connected to ground potential of the PCB	GND
P89	PCIE_A_TX+	I DP (PCIE)	Differential PCIe link A transmit data pair	J16 (M.2 Key-A)
P90	PCIE_A_TX-			
P91	GND	GND	Connected to ground potential of the PCB	GND
P92	HDMI_D2+/DP1_LANE0+	I DP (TMDS)	Secondary DP port differential Pair Data Lines	DisplayPort Mode.
P93	HDMI_D2-/DP1_LANE0-			USB Type-C or Vx1
P94	GND	GND	Connected to ground potential of the PCB	GND
P95	HDMI_D1+/DP1_LANE1+	I DP (TMDS)	Secondary DP port differential Pair Data Lines	DisplayPort Mode.
P96	HDMI_D1-/DP1_LANE1-			USB Type-C or Vx1
P97	GND	GND	Connected to ground potential of the PCB	GND
P98	HDMI_D0+/DP1_LANE2+	I DP (TMDS)	Secondary DP port differential Pair Data Lines	DisplayPort Mode.
P99	HDMI_D0-/DP1_LANE2-			USB Type-C or Vx1
P100	GND	GND	Connected to ground potential of the PCB	GND
P101	HDMI_CK+/DP1_LANE3+	I DP (TMDS)	Secondary DP port differential Pair Data Lines	DisplayPort Mode.
P102	HDMI_CK-/DP1_LANE3-			USB Type-C or Vx1
P103	GND	GND	Connected to ground potential of the PCB	GND
P104	HDMI_HPD/DP1_HPD	I (CMOS 1.8V)	HDMI Hot Plug Active High Detection	USB Type-C or Vx1
P105	HDMI_CTRL_CK/DP1_AUX+	I (TMDS)	Secondary DP Port Bidirectional Channel used	DisplayPort Mode.
P106	HDMI_CTRL_DAT/DP1_AUX-		for Link Management and Device Control	USB Type-C or Vx1
P107	DP1_AUX_SEL	O (CMOS 1.8V)	Tied to GND	GND = AUX mode
P108	GPIO0/CAM0_PWR#	IO (CMOS1.8V)	General purpose IO	J51 over LS to 3.3V
P109	GPIO1/CAM1_PWR#	IO (CMOS1.8V)	General purpose IO	J51 over LS to 3.3V
P110	GPIO2/CAM0_RST#	IO (CMOS1.8V)	General purpose IO	J51 over LS to 3.3V
P111	GPIO3/CAM1_RST#	IO (CMOS1.8V)	General purpose IO	J51 over LS to 3.3V
P112	GPIO4/HDA_RST#	I (CMOS1.8V)	General purpose IO / HD-Audio Reset	J51 over LS to 3.3V or HDA Codec
P113	GPIO5/PWM_OUT	IO (CMOS1.8V)	General purpose IO	J51 over LS to 3.3V
P114	GPIO6/TACHIN	IO (CMOS1.8V)	General purpose IO	J51 over LS to 3.3V
P115	GPIO7	IO (CMOS1.8V)	General purpose IO	J51 over LS to 3.3V
P116	GPIO8	IO (CMOS1.8V)	General purpose IO	Board Controller STM32
P117	GPIO9	IO (CMOS1.8V)	General purpose IO	Board Controller STM32
P118	GPIO10	IO (CMOS1.8V)	General purpose IO	Board Controller STM32

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
P119	GPIO11	IO (CMOS1.8V)	General purpose IO	Board Controller STM32
P120	GND	GND	Connected to ground potential of the PCB	GND
P121	I2C_PM_CK	IO (CMOS 1.8V/3.3V)	Power management I2C bus Clock	See I2C topology
P122	I2C_PM_DAT	IO (CMOS 1.8V/3.3V)	Power management I2C bus Data	See I2C topology
P123	BOOT_SEL0#	O (OD1.8V)	Input straps determine the module boot device.	J44
P124	BOOT_SEL1#			
P125	BOOT_SEL2#			
P126	RESET_OUT#	I (CMOS 1.8V)	General purpose reset output to Carrier Board.	CB_RESET#
P127	RESET_IN#	O OD (CMOS 1.8V)	Reset output to SMARC module.	Board Controller STM32
P128	POWER_BTN#	O OD (CMOS 1.8V to5V)	Power-Button output to SMARC module.	Board Controller STM32
P129	SER0_TX	I (CMOS 1.8V)	Asynchronous serial data output port 0	J47 (UART CMOS)
P130	SER0_RX	O (CMOS 1.8V)	Asynchronous serial data input port 0	J47 (UART CMOS)
P131	SER0_RTS#	I (CMOS 1.8V)	Request to send handshake line for port 0	J47 (UART CMOS)
P132	SER0_CTS#	O (CMOS 1.8V)	Clear to send handshake line for port 0	J47 (UART CMOS)
P133	GND	GND	Connected to ground potential of the PCB	GND
P134	SER1_TX	I (CMOS 1.8V)	Asynchronous serial data output port 1	J48 (UART CMOS)
P135	SER1_RX	O (CMOS 1.8V)	Asynchronous serial data input port 1	J48 (UART CMOS)
P136	SER2_TX	I (CMOS 1.8V)	Asynchronous serial data output port 2	J50 (RS485)
P137	SER2_RX	O (CMOS 1.8V)	Asynchronous serial data input port 2	J50 (RS485)
P138	SER2_RTS#	I (CMOS 1.8V)	Request to send handshake for SER port 2	RS485 direction control
P139	SER2_CTS#	O (CMOS 1.8V)	Clear to send handshake line for port 2	Not connected on CB
P140	SER3_TX	I (CMOS 1.8V)	Asynchronous serial data output port 3	J49 (RS232)
P141	SER3_RX	O (CMOS 1.8V)	Asynchronous serial data input port 3	J49 (RS232)
P142	GND	GND	Connected to ground potential of the PCB	GND
P143	CAN0_TX	I (CMOS 1.8V)	CAN Port 0 transmit output	J41 (over MCP5262)
P144	CAN0_RX	O (CMOS 1.8V)	CAN Port 0 recive input	J41 (over MCP5262)
P145	CAN1_TX	I (CMOS 1.8V)	CAN Port 1 transmit output	not connected on CB
P146	CAN1_RX	O (CMOS 1.8V)	CAN Port 1 recive input	not connected on CB
P147	VDD_IN	Power 5V (+/-5%)	Main power supply to SMARC module maximum current 3A.	V_5V0_REG
P148	VDD_IN			
P149	VDD_IN			
P150	VDD_IN			
P151	VDD_IN			
P152	VDD_IN			
P153	VDD_IN			
P154	VDD_IN			
P155	VDD_IN			
P156	VDD_IN			

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
S1	CSI1_TX+/I2C_CAM1_CK	IO / DP	I2C CSI camera support or DP data lane	not connected on CB
S2	CSI1_TX-/I2C_CAM1_DAT	IO / DP	I2C CSI camera support or DP data lane	not connected on CB
S3	GND	GND	Connected to ground potential of the PCB	GND
S4	RSVD	RSVD	NC	not connected on CB
S5	CSI0_TX+/I2C_CAM0_CK	IO / DP	I2C CSI camera support or DP data lane	not connected on CB
S6	CAM_MCK	I (CMOS 1.8V)	Master Clock Input for Camera Interface	not connected on CB
S7	CSI0_TX-/I2C_CAM0_DAT	IO / DP	I2C CSI camera support or DP data lane	not connected on CB
S8	CSI0_CK+	O DP (D-PHY)	CSI0 differential data output	not connected on CB
S9	CSI0_CK-			
S10	GND	GND	Connected to ground potential of the PCB	GND
S11	CSI0_RX0+	O DP (D-PHY)	CSI0 differential data output	not connected on CB
S12	CSI0_RX0-			
S13	GND	GND	Connected to ground potential of the PCB	GND
S14	CSI0_RX1+	O DP (D-PHY)	CSI0 differential data output	not connected on CB
S15	CSI0_RX1-			
S16	GND	GND	Connected to ground potential of the PCB	GND
S17	GBE1_MDI0+	IO DP (GBE MDI)	Differential pair signals for external transformer	J35 (RJ45)
S18	GBE1_MDI0-			
S19	GBE1_LINK100#	I OD (CMOS 3.3V)	Link speed indication LED for GBE1 100Mbps	J35 (RJ45)
S20	GBE1_MDI1+	IO DP (GBE MDI)	Differential pair signals for external transformer	J35 (RJ45)
S21	GBE1_MDI1-			
S22	GBE1_LINK1000#	I OD (CMOS 3.3V)	Link speed indication LED for GBE1 1000Mbps	J35 (RJ45)
S23	GBE1_MDI2+	IO DP (GBE MDI)	Differential pair signals for external transformer	J35 (RJ45)
S24	GBE1_MDI2-			
S25	GND	GND	Connected to ground potential of the PCB	GND
S26	GBE1_MDI3+	IO DP (GBE MDI)	Differential pair signals for external transformer	J35 (RJ45)
S27	GBE1_MDI3-			
S28	GBE1_CTREF	Analog (0 to 3.3V)	Center-tap ref. Voltage for GBE1 magnetic	J35 (RJ45)
S29	PCIE_D_TX+	I DP (PCIE)	Differential PCIe link D transmit data pair	not connected on CB
S30	PCIE_D_TX-			
S31	GBE1_LINK_ACT#	I OD (CMOS 3.3V)	Link / activity indication for GBE1	J35 (RJ45)
S32	PCIE_D_RX+	O DP (PCIE)	Differential PCIe link D receive data pair	not connected on CB
S33	PCIE_D_RX-			
S34	GND	GND	Connected to ground potential of the PCB	GND
S35	USB4+	IO DP	USB differential data pairs for port 4	J16 (M.2 Key-A)
S36	USB4-			
S37	USB3_VBUS_DET	USB (VBUS 5V)	USB Port 3 host power detection	not connected on CB

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
S38	AUDIO_MCK	I (CMOS 1.8V)	Master clock output to I2S codec(s)	optional to Y4
S39	I2S0_LRCK	IO (CMOS 1.8V)	I2S0 left & right synchronization clock	I2S Audio Codec
S40	I2S0_SDOUT	I (CMOS 1.8V)	I2S0 digital audio output from module	I2S Audio Codec
S41	I2S0_SDIN	O (CMOS 1.8V)	I2S0 digital audio input to module	I2S Audio Codec
S42	I2S0_CK	IO (CMOS 1.8V)	I2S0 left & right synchronization clock	I2S Audio Codec
S43	ESPI_ALERT0#	O (OD CMOS 1.8V)	ESPI ALERT to module	not connected on CB
S44	ESPI_ALERT1#	O (OD CMOS 1.8V)	ESPI ALERT to module	not connected on CB
S45	MDIO_CLK	I (OD CMOS 1.8V)	MDIO signals to configure possible PHYs	not connected on CB
S46	MDIO_DAT	IO(OD CMOS 1.8V)	MDIO signals to configure possible PHYs	not connected on CB
S47	GND	GND	Connected to ground potential of the PCB	GND
S48	I2C_GP_CK	I (CMOS 1.8V)	General purpose I2C clock signal	See I2C topology
S49	I2C_GP_DAT	IO (CMOS 1.8V)	General purpose I2C data signal	See I2C topology
S50	HDA_SYNC	IO(CMOS 1.5/1.8V)	HDA Sample synchronization clock to codec	HDA-Codec
S51	HDA_SDO	I(CMOS 1.5/1.8V)	HDA data to codec	HDA-Codec
S52	HDA_SDI	O(CMOS 1.5/1.8V)	HDA data from codec	HDA-Codec
S53	HDA_CK	I(CMOS 1.5/1.8V)	HDA clock to codec	HDA-Codec
S55	USB5_EN_OC#	IO (OD CMOS 3.3V)	USB over-current sense and power enable port 5	not connected on CB
S56	ESPI_IO_2/QSPI_IO_2	IO (CMOS 1.8V)	SPI1 IO2 or write protect#	J43
S57	ESPI_IO_3/QSPI_IO_3	IO (CMOS 1.8V)	SPI1 IO3 or SPI hold (low active)	J43
S58	ESPI_RESET#	IO (CMOS 1.8V)	ESPI reset	not connected on CB
S59	USB5+	IO DP	USB differential data pairs for port 5	J18 (M.2 Key-B)
S60	USB5-			
S61	GND	GND	Connected to ground potential of the PCB	GND
S62	USB3_SSTX+	O DP (USB SS)	Transmit signal differential pairs for SuperSpeed on Port 3 from module	J24 (lower port)
S63	USB3_SSTX-			
S64	GND	GND	Connected to ground potential of the PCB	GND
S65	USB3_SSRX+	I DP (USB SS)	Receive signal differential pairs for	J24 (lower port)
S66	USB3_SSRX-		SuperSpeed on port 3 to module	
S67	GND	GND	Connected to ground potential of the PCB	GND
S68	USB3+	IO DP	USB differential data pairs for port 3	J24 (lower port)
S69	USB3-			
S70	GND	GND	Connected to ground potential of the PCB	GND
S71	USB2_SSTX+	I DP (USB SS)	Transmit signal differential pairs for SuperSpeed on port 2 from module	USB Type-C or
S72	USB2_SSTX-			J24 (upper port)
S73	GND	GND	Connected to ground potential of the PCB	GND

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
S74	USB2_SSRX+	O DP (USB SS)	Receive signal differential pairs for	USB Type-C or
S75	USB2_SSRX-		SuperSpeed on port 2 to module	J24 (upper port)
	Key			
S54	SATA_ACT#	O (OD 3.3V)	SATA activity indicator (>24mA)	SATA Act. LED
S76	PCIE_B_RST#	I (CMOS 3.3V)	PCIe port B reset input	J18 (M.2 Key-B)
S77	PCIE_C_RST#	I (CMOS 3.3V)	PCIe port C reset input	USB3.0 Controller
S78	PCIE_C_RX+	O DP (PCIE)	Differential PCIe link C receive data pair	USB3.0 Controller
S79	PCIE_C_RX-			
S80	GND	GND	Connected to ground potential of the PCB	GND
S81	PCIE_C_TX+	I DP (PCIE)	Differential PCIe link C transmit data pair	USB3.0 Controller
S82	PCIE_C_TX-			
S83	GND	GND	Connected to ground potential of the PCB	GND
S84	PCIE_B_REFCK+	I DP (PCIE)	Differential PCIe link B reference	J18 (M.2 Key-B)
S85	PCIE_B_REFCK-		clock input	
S86	GND	GND	Connected to ground potential of the PCB	GND
S87	PCIE_B_RX+	O DP (PCIE)	Differential PCIe link C receive data pair	USB3.0 Controller
S88	PCIE_B_RX-			
S89	GND	GND	Connected to ground potential of the PCB	GND
S90	PCIE_B_TX+	I DP (PCIE)	Differential PCIe link B receive data pair	J18 (M.2 Key-B)
S91	PCIE_B_TX-			
S92	GND	GND	Connected to ground potential of the PCB	GND
S93	DP0_LANE0+	I DP (TMDS)	Primary DP port differential	J28 DisplayPort
S94	DP0_LANE0-		Pair Data Lines	(IO Shield)
S95	DP0_AUX_SEL	O (CMOS 3.3V)	Auxiliary selection	J28 DisplayPort
S96	DP0_LANE1+	I DP (TMDS)	Primary DP port differential pair data lines	J28 DisplayPort
S97	DP0_LANE1-			(IO Shield)
S98	DP0_HPD	O (CMOS 1.8V)	DP hot plug detect Input	J28 DisplayPort
S99	DP0_LANE2+	I DP (TMDS)	Primary DP port differential pair data lines	J28 DisplayPort
S100	DP0_LANE2-			(IO Shield)
S101	GND	GND	Connected to ground potential of the PCB	GND
S102	DP0_LANE3+	I DP (TMDS)	Primary DP port differential pair data lines	J28 DisplayPort
S103	DP0_LANE3-			(IO Shield)
S104	USB3_OTG_ID	O (CMOS 3.3V)	Output to indicate OTG Device Insertion on Port 3	not connected on CB
S105	DP0_AUX+	IO DP (LVDS)	Primary DP port bidirectional channel used for link management and device control	J28 DisplayPort
S106	DP0_AUX-			(IO Shield)
S107	LCD1_BKLT_EN	I (CMOS 1.8V)	Secondary LVDS Channel Backlight Enable	not connected on CB
S108	LVDS1_CK+	I DP (LVDS)	Secondary LVDS channel diff. pair clock lines	J30
S109	LVDS1_CK-			
S110	GND	GND	Connected to ground potential of the PCB	GND
S111	LVDS1_0+	I DP (LVDS)	Secondary LVDS channel diff. pair data lines	J30
S112	LVDS1_0-			

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
S113	eDP1_HPD/DSI1_TE	O (CMOS 1.8V)	Detection of Hot Plug / Unplug of Secondary eDP Display and Notification of the Link Layer	10k PD to GND
S114	LVDS1_1+	I DP (LVDS)	Secondary LVDS channel diff. pair data lines	J30
S115	LVDS1_1-			
S116	LCD1_VDD_EN	I (CMOS 1.8V)	Secondary LVDS Channel Power Enable	not connected on CB
S117	LVDS1_2+	I DP (LVDS)	Secondary LVDS channel diff. pair data lines	J30
S118	LVDS1_2-			
S119	GND	GND	Connected to ground potential of the PCB	GND
S120	LVDS1_3+	I DP (LVDS)	Secondary LVDS channel diff. pair data lines	J30
S121	LVDS1_3-			
S122	LCD1_BKLT_PWM	I (CMOS 1.8V)	Secondary LVDS Channel Brightness Control	not connected on CB
S123	GPIO13	IO (CMOS 1.8V)	Genera Purpose IO	not connected on CB
S124	GND	GND	Connected to ground potential of the PCB	GND
S125	LVDS0_0+	I DP (LVDS)	Primary LVDS channel diff. pair data lines	J30
S126	LVDS0_0-			
S127	LCD0_BKLT_EN	I (CMOS 1.8V)	Primary LVDS Channel Backlight Enable	J29
S128	LVDS0_1+	I DP (LVDS)	Primary LVDS channel diff. pair data lines	J30
S129	LVDS0_1-			
S130	GND	GND	Connected to ground potential of the PCB	GND
S131	LVDS0_2+	I DP (LVDS)	Primary LVDS channel diff. pair data lines	J30
S132	LVDS0_2-			
S133	LCD0_VDD_EN	I (CMOS 1.8V)	Primary LVDS channel power enable	J30
S134	LVDS0_CK+	I DP (LVDS)	Primary LVDS channel diff. pair clock lines	J30
S135	LVDS0_CK-			
S136	GND	GND	Connected to ground potential of the PCB	GND
S137	LVDS0_3+	I DP (LVDS)	Primary LVDS channel diff. pair data lines	J30
S138	LVDS0_3-			
S139	I2C_LCD_CK	I (CMOS 1.8V)	I2C clock to read LCD display EDID EEPROMs	See I2C topology
S140	I2C_LCD_DAT	IO (CMOS 1.8V)	I2C Data to Read LCD Display EDID EEPROMs	See I2C topology
S141	LCD0_BKLT_PWM	I (CMOS 1.8V)	Primary LVDS Channel Brightness Control	J29
S142	GPIO12	IO (CMOS 1.8V)	General purpose IO	not connected on CB
S143	GND	GND	Connected to ground potential of the PCB	GND
S144	eDP0_HPD/DSI0_TE	O (CMOS 1.8V)	Detection of hot plug / unplug of primary eDP display and notification of the link layer	10k PD to GND
S145	WDT_TIME_OUT#	I (CMOS 1.8V)	Watch-dog-timer output, low active	J51 LS to 3.3V (Feature Connector)
S146	PCIE_WAKE#	IO (CMOS 1.8V)	PCIe wake up interrupt to host – common to PCIe links A, B, C, D	PCIE Devices and Board Controller STM32
S147	VDD_RTC	Analog (2.0 to 3.3V)	Low current RTC circuit backup power – 3.0V nominal	RTC Battery

Pin	Signal / Function	Pin Type	Signal Description	Device/Connection
S148	LID#	O OD (CMOS 1.8 to 5V)	Lid open/close indication to Module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.	J51 LS to 3.3V (Feature Connector)
S149	SLEEP#	O OD (CMOS 1.8 to 5V)	Sleep indicator from carrier board. May be sourced from user sleep button or carrier logic. Carrier to float the line in in-active state. Active low. level sensitive. Should be de-bounced on the Module.	J51 LS to 3.3V (Feature Connector)
S150	VIN_PWR_BAD#	O OD (VDD_IN)	Power bad indication from CB. Module and Carrier power supplies (other than module and carrier power supervisory circuits) shall not be enabled while this signal is held low by the carrier.	Board Controller STM32
S151	CHARGING#	O OD (CMOS 1.8 to 5V)	Held low by CB during battery charging. Carrier to float the line when charge is complete.	not connected on CB
S152	CHARGER_PRSNT#	O OD (CMOS 1.8 to 5V)	Held low by CB if DC input for battery charger is present.	not connected on CB
S153	CARRIER_STBY#	I (CMOS 1.8V)	The module drives this signal low when the system is in a standby power state.	Board Controller STM32
S154	CARRIER_PWR_ON	I (CMOS 1.8V)	Carrier Board circuits (apart from power management and power path circuits) are not powered up until the module asserts the CARRIER_PWR_ON signal.	Board Controller STM32
S155	FORCE_RECOV#	O OD (CMOS 1.8V)	Low on this pin allows non-protected segments of Module boot device to be re-written / restored from an external USB host on Module USB0. The module USB0 operates in Client Mode when in the force recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based force recovery functions, then a low on the module FORCE_RECOV# pin may invoke the SOC native force recovery mode – such as over a serial port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on module. Driven by OD part on carrier.	J44
S156	BATLOW#	O OD (CMOS 1.8 to 5V)	Battery low indication to module. Carrier to float the line in inactive state.	not connected on CB
S157	TEST#	O OD (CMOS 1.8 to 5V)	Held low by carrier to Invoke module vendor specific test functions.	Test point TP313
S158	GND	GND	Connected to ground potential of the PCB	GND

4.2. Power IN Supply Voltage Connector

Reference Designator: J2

Description

J2 is a 24V main power supply connector of the carrier board. The connector is an ATX-P4 compliant straight header, THT delivering 24V (instead of 12V as defined by ATX).
There is no overcurrent protection foreseen on the eDM-CB-SM-IPCS for power-supply input.
The **12A** maximum current must be limited by the power supply unit!

Connector drawing and contact-numbering scheme

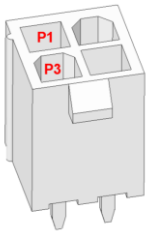


Figure 11 Power In Connector

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J2	1	GND	GND	Main power supply ground terminal
	2	GND		
	3	V_IN	Power (24V)	24V (+/- 5%) Main power supply connection terminal
	4	V_IN		

4.3. M.2 Key A Connector

Reference Designator: J16

Description

M.2 key A compliant socket connector with mounting holes to support card sizes 2230, 3030 and 3042.
The J16 provides PCIe and USB only (no DP, SDIO or UART).

Interfaces used

PCI Express port A (single lane)
USB 2.0 port 4 of the SMARC module
I2C (optional)

Mechanic

Mounting Holes to hold solder-in standoff for M3 screw in position for 30mm and 42mm card length
Default assembly at 30mm position

Connector drawing and contact-numbering scheme

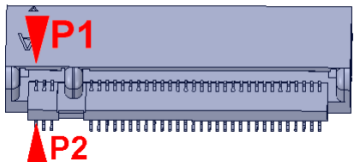


Figure 12 M.2 Key A Connector – J16

Pinout

PCIe and USB only (no DP, SDIO or UART), according to PCI Express M.2 specification revision 1.1 table 22 and 23

4.4. M.2 Key B Connector

Reference Designator: J18

Description

M.2 key B compliant socket connector with mounting holes to support card size 3042

Interfaces used

PCI Express port B (single lane)
USB 2.0 port 5 of the SMARC module
One UIM Interface for SIM cards

Mechanic

Mounting Holes to hold solder-in standoff for M3 screw in position for 42mm card length

Connector drawing and contact-numbering scheme

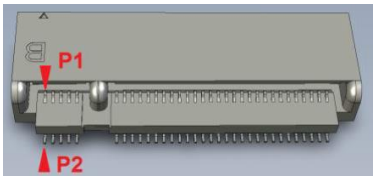


Figure 13 M.2 Key B Connector – J18

Pinout

PCIe and USB only, according to PCI Express M.2 specification revision 1.1

4.5. Nano-SIM Connector

Reference Designator: J17

Description

Nano-SIM socket with push-push card support. The J17 can only be used in combination with M.2 Key-B extension cards.

Interfaces used

UIM1 of the M.2 key B socket

Connector drawing and contact-numbering scheme

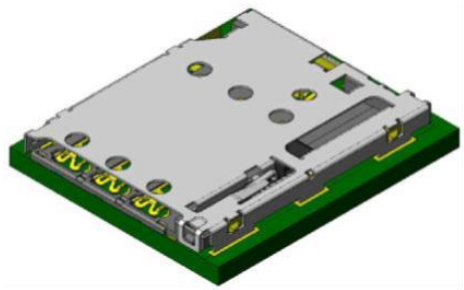


Figure 14 Nano-SIM Connector– J17

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J17	C1	UIM_PWR	Power	Device power (provided by M.2 Key B device)
	C2	UIM_RESET	I	Device reset
	C3	UIM_CLK	I	Data clock
	C5	GND	GND	Connected to ground potential of the PCB
	C6	n. c. (optional UIM_PWR)	NC	not connected
	C7	UIM_DATA	IO	Data Line
	DETECT1	UIM_SIM-DETECT	O	Device presence indication
	DETECT2	GND	GND	Connected to ground potential of the PCB

4.6. M.2 Key M Connector

Reference Designator: J19

Description

The J19 is a standard M2.0 Key-M connector, which provides SATA0 interface of the SMARC module. The data transfer performance is depended on the SATA controller of the SMARC module. The SATA0 interface is shared with 7-pin L-shape SATA connector J20. See more details in chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

SATA Port 0 (shared with 7-pin SATA socket J20)

Pinout

SATA according to PCI Express M.2 Specification Revision 1.1 table 33

Mechanic

Mounting Holes to hold solder-in standoff for M3 screw in position for 42mm card length

Connector drawing and contact-numbering scheme

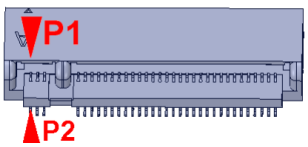


Figure 15 M.2 Key M Connector – J19

4.7. SATA 7-Pin Connector

Reference Designator: J20

SATA 7 pin male straight connector (Nexus 3504AFT)

Description

The J20 is a standard 7-pin L-shape SATA connector, which provides SATA0 Interface of the SMARC module. The data transfer performance is depended on the SATA controller of the SMARC module. The SATA0 interface is shared with M2.0 Key-M socket J19. See more details in chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

SATA Port 0 (shared with M.2 Key-M socket J19)

Connector drawing and contact-numbering scheme

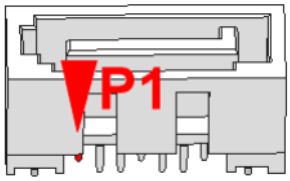


Figure 16 SATA Connector – J20

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J20	1	GND	GND	Connected to ground potential of the PCB
	2	SATA0_TX_P	O	pos. signal of the differential TX datapair
	3	SATA0_TX_N	O DP	neg. signal of the differential TX datapair
	4	GND	GND	Connected to ground potential of the PCB
	5	SATA0_RX_N	I DP	neg. signal of the differential RX datapair
	6	SATA0_RX_P	I DP	pos. signal of the differential RX datapair
	7	GND	GND	Connected to ground potential of the PCB

4.8. USB 2.0 Port 1D on Molex PicoBlade

Reference Designator: J23

1.25mm Pitch Molex PicoBlade Wire-to-board header, SMT, straight, 4 circuits

Description

The J23 USB2.0 internal PicoBlade pin-header provides one USB2.0 Ports of the Hub USB2514B. The USB2514B uplink port is connected to the USB2.0 port 1 of the SMARC module. The downstream ports 1D of the USB Hub is connected to the J21. The port 1D is shared with uplink port of USB Hub (USB2.0 Port 1 of the SMARC module) . See more details in chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

USB 2.0 port 1D provided by the USB- Hub

Connector drawing and contact-numbering scheme

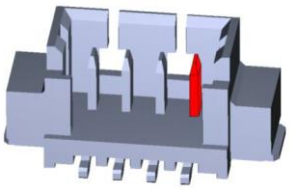


Figure 17 USB2.0 PicoBlade – J23

Pinout according to Data Modul Inhouse-Standard DMIS05

	Pin	Signal / Function	Pin Type	Signal Description
J23	1	VCC	Power 5.0V (S5)	5V power-supply for USB device; max. current: 100 mA
	2	USB2_1D_P (optional USB2_1_P)	IO DP	pos. signal of the differential 1D datapair
	3	USB2_1D_N (optional USB2_1_N)	IO DP	neg. signal of the differential 1D datapair
	4	GND	GND	USB device power ground

4.9. USB 2.0 Port 1B/C on 9-pin Pin-header

Reference Designator: J21

2.54mm Pitch Pin-header, THT, straight, 10 circuits with removed 9th pin

Description

The J25 standard USB2.0 internal pin-header provides two USB2.0 ports via USB2.0 Hub USB2514B.The USB2514B uplink port is connected to the USB2.0 port 1 of the SMARC module.
Two downstream ports 1B and 1C of the USB Hub are connected to the J21. The downstream port 1B is shared with upper port of J22 (USB2.0 Type-A). See more details in chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

USB 2.0 port 1B and 1C of the USB hub
Supplied by 5V S5 voltage (V_5V0_S5)
Current limited to 500 mA per port

Reference Designator: J21

2.54mm Pitch Pin-header, THT, straight, 10 circuits with removed 9th pin

Connector drawing and contact-numbering scheme

Figure 18 USB2.0 Pin-header – J21

Pinout according to Data Modul Inhouse-Standard DMIS15

	Pin	Signal / Function	Pin Type	Signal Description
J21	1	V_5V0_S5_USB1B	Power (5V)	5V/500mA power-supply for device 1B
	2	V_5V0_S5_USB1C	Power (5V)	5V/500mA power-supply for device 1C
	3	USB2_1B_N	IO DP	neg. signal of the differential 1B datapair
	4	USB2_1C_N	IO DP	neg. signal of the differential 1C datapair
	5	USB2_1B_P	IO DP	pos. signal of the differential 1B datapair
	6	USB2_1C_P	IO DP	pos. signal of the differential 1C datapair
	7	GND_USB1B	GND	Power ground for port 1B
	8	GND_USB1C	GND	Power ground for port 1C
	9	Not available (KEY)	n/a	removed pin (Key)
	10	NC	n/a	not connected

4.10. USB 3.0 19-pin Pin-header

Reference Designator: J25

2.0mm Pitch Pin-header, THT, straight, 19 circuits

Description

The J25 standard USB3.0 internal pin-header provides two USB3.0 ports via PCIexpress to USB3.0 Bridge TUSB7320. The TUSB7320 is connected to PCIe Lane “C” of the SMARC module.

Interfaces used

USB 2.0 port 6 and 7 of the USB controller
USB 3.0 port 6 and 7 of the USB controller
Supplied by 5V S0 voltage (V_5V0_S0). Current limited to 0.9 A per port

Connector drawing and contact-numbering scheme

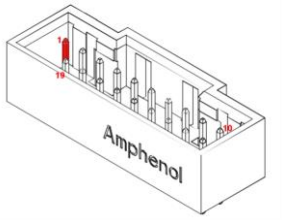


Figure 19 USB2.0 Pin-header – J25

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J25	1	V_5V0_S0_USB6	Power (5V)	5V/900mA power-supply for device 6
	2	USB_SSRX6_N	I DP	neg. signal of the differential Port 6 RX datapair
	3	USB_SSRX6_P	I DP	pos. signal of the differential Port 6 RX datapair
	4	GND_USB6	GND	Power ground for port 6
	5	USB_SSTX6_N	O DP	neg. signal of the differential Port 6 TX datapair
	6	USB_SSTX6_P	O DP	pos. signal of the differential Port 6 TX datapair
	7	GND_USB6	GND	Power ground for port 6
	8	USB2_6_N	IO DP	neg. signal of the differential Port 6 datapair
	9	USB2_6_P	IO DP	pos. signal of the differential Port 6 datapair
	10	ID	NC	n/a
	11	USB2_7_P	IO DP	pos. signal of the differential Port 7 datapair
	12	USB2_7_N	IO DP	neg. signal of the differential Port 7 datapair
	13	GND_USB7	GND	Power ground for port 7
	14	USB_SSTX7_P	O DP	pos. signal of the differential Port 7 TX datapair
	15	USB_SSTX7_N	O DP	neg. signal of the differential Port 7 TX datapair
	16	GND_USB7	GND	Power ground for port 7
	17	USB_SSRX7_P	O DP	pos. signal of the differential Port 7 RX datapair
	18	USB_SSRX7_N	O DP	neg. signal of the differential Port 7 RX datapair
	19	V_5V0_S0_USB7	Power (5V)	5V/900mA power-supply for device 6
	20	Key (removed pin)	Key	n/a

4.11. SPI0 Socket / Pin-header

Reference Designator: J42

Description

The J42 connector can be optionally sampled either by Lotes SPI Flash socket (PN: ACA-SPI-004-K01) or SOIC 8PIN 200Mils (BIOS-flash) or an 8-pin 1.27mm SMT pin-header.

Interfaces used

Boot- SPI0 Interface from the SMARC module, **CMOS 1.8V** signal characteristics

Reference Designator: J42

Connector drawing and contact-numbering scheme

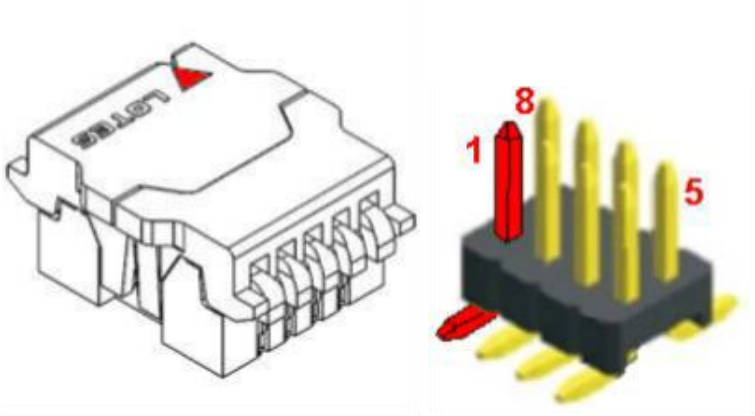


Figure 20 SPI socket / pin-header – J42

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J42	1	SPI0_CS#	I (CMOS 1.8V)	Chip select input
	2	SPI0_MISO	O (CMOS 1.8V)	Slave data output
	3	SPI0_WP#	IO (CMOS 1.8V)	Device write protection
	4	GND	GND	Connected to ground potential of the PCB
	5	SPI0_MOSI	I (CMOS 1.8V)	Slave data input
	6	SPI0_CLK	I (CMOS 1.8V)	Serial clock input
	7	SPI0_HOLD#	IO (CMOS 1.8V)	Hold or reset input
	8	VCC	Power 1.8V (S5)	Power supply for attached device; max. current 25mA.

4.12. SPI0 Socket / Pin-header

Reference Designator: J43

Description

The J43 connector provides SPI1 interface of the SMARC module to an 8-pin 1.27mm SMT pin-header.

Interfaces used

SPI1 Interface of the SMARC module, **CMOS 1.8V** signal characteristics

Connector drawing and contact-numbering scheme

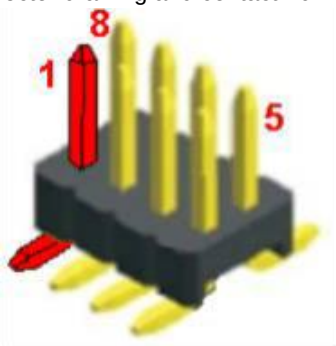


Figure 21 SPI socket / pin-header – J43

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J43	1	SPI1_CS#	I (CMOS 1.8V)	Chip select input
	2	SPI1_MISO	O (CMOS 1.8V)	Slave data output
	3	SPI1_IO2	IO (CMOS 1.8V)	Device write protection
	4	GND	GND	Connected to ground potential of the PCB
	5	SPI1_MOSI	I (CMOS 1.8V)	Slave data input
	6	SPI1_CLK	I (CMOS 1.8V)	Serial clock input
	7	SPI1_IO3	IO (CMOS 1.8V)	Hold or reset input
	8	VCC	Power 1.8V (S5)	Power supply for attached device; max. current 25mA.

4.13. UART SER0 Connector

Reference Designator: J47

1.25mm Pitch Molex PicoBlade Wire-to-board header, SMT, straight, 6 circuits

Description

The J47 connector provides SER0 UART inclusive RTS/CTS handshake signals of the SMARC module for internal device communication.

Interfaces used

SER1 from SMARC module, direct **CMOS 1.8V** signal characteristics

Connector drawing and contact-numbering scheme

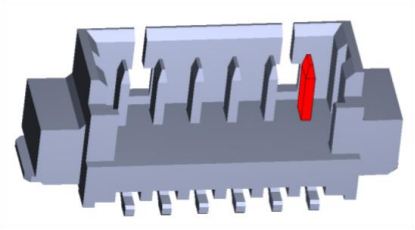


Figure 22 Connector – J47

Pinout according to Data Modul Inhouse-Standard DMIS07

	Pin	Signal / Function	Pin Type	Signal Description
J47	1	VCC	Power 5.0V(S0)	Power supply for attached device; max. current 200mA
	2	GND	GND	Connected to ground potential of the PCB
	3	CTS#	I (CMOS 1.8V)	Clear to send
	4	TXD	O (CMOS 1.8V)	Transmit data
	5	RTS#	O (CMOS 1.8V)	Request to send
	6	RXD	I (CMOS 1.8V)	Receive Data

4.14. UART SER1 Connector

Reference Designator: J48

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 6 circuits

Description

The J48 connector provides SER1 UART (Rx/Tx only) of the SMARC module for internal device communication.

Interfaces used

SER1 from SMARC module, direct **CMOS 1.8V** signal characteristics

Connector drawing and contact-numbering scheme

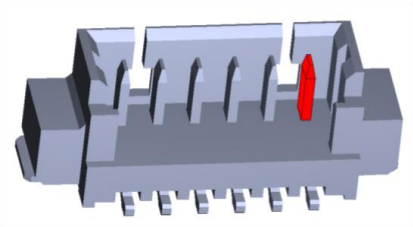


Figure 23 Connector – J48

Pinout according to Data Modul Inhouse-Standard DMIS08

	Pin	Signal / Function	Pin Type	Signal Description
J48	1	VCC	Power 5.0V(S0)	Power supply for attached device; max. current 200mA
	2	GND	GND	Connected to ground potential of the PCB
	3	unconnected	NC	not connected
	4	TXD (CMOS 1.8V)	O (CMOS 1.8V)	Transmit data
	5	unconnected	NC	not connected
	6	RXD (CMOS 1.8V)	I (CMOS 1.8V)	Receive data

4.15. RS485 (SER2) Connector

Reference Designator: J50

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 4 circuits

Description

The J50 connector provides SER2 UART of the SMARC module over MAX3443E RS485 transceiver.

Interfaces used

SER2 of the SMARC module converted to RS485

Connector drawing and contact-numbering scheme

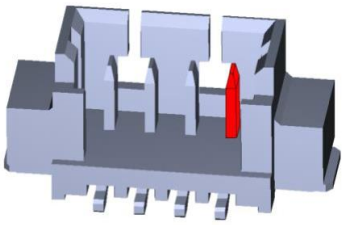


Figure 24 Connector – J50

Pinout according to Data Modul Inhouse-Standard DMIS09

	Pin	Signal / Function	Pin Type	Signal Description
J50	1	VCC	Power 5.0V(S0)	Power supply for attached device; max. current 200mA
	2	RS485_N	IO DP	Neg. signal of the differential RS485 datapair
	3	RS485_P	IO DP	Pos. signal of the differential RS485 datapair
	4	GND	GND	Connected to ground potential of the PCB

4.16. RS232 (SER3) Connector

Reference Designator: J49

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 6 circuits

Description

The J49 connector provides SER3 UART of the SMARC module over MAX3232E RS232 transceiver.

Interfaces used

SER3 of the SMARC converted to RS232

Connector drawing and contact-numbering scheme

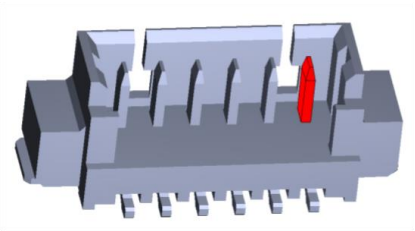


Figure 25 Connector – J49

Pinout according to Data Modu Inhouse-Standard DMIS07

	Pin	Signal / Function	Pin Type	Signal Description
J49	1	VCC	Power 5.0V(S0)	Power supply for attached device; max. current 200mA
	2	GND	GND	Connected to ground potential of the PCB
	3	Not Connected	NC	Not connected
	4	TXD (RS232)	O (RS232)	Transmit Data
	5	Not Connected	NC	Not connected
	6	RXD (RS232)	I (RS232)	Receive Data

4.17. I2S Audio Microphone

Reference Designator: J39

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 6 circuits

Description

This connector provides I2S Interface to drive I2S Digital Microphone like Adafruit SPH0645 I2S MEMS.
Used I2S Interface is shared with I2S Codec (WM8904). See more details in chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

I2S0 (shared with I2S Audio Codec) port from the SMARC module, direct CMOS 1.8V signal characteristics.

Connector drawing and contact-numbering scheme

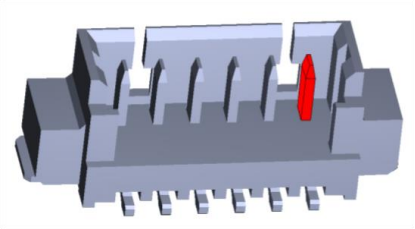


Figure 26 Connector – J39

Pinout matching Adafruit SPH0645 I2S MEMS microphone pinout

	Pin	Signal / Function	Pin Type	Signal Description
J39	1	VCC	Power 1.8V(S0)	Microphone Power Supply; max. current 100mA
	2	GND	GND	Power ground
	3	I2S0_CLK (CMOS 1.8V)	O	Master clock
	4	I2S0_SDIN (CMOS 1.8V)	I	Serial Audio Data Input
	5	I2S0_LRCK (CMOS 1.8V)	I	Left/Right Clock Determination for SDIN
	6	SEL (CMOS 1.8V)	O	Default: Pulled down with 100k Ohm resistor on CB Opt: assembly-position for pull-up resistor to VCC 1.8 (S0)

4.18. Audio Frontpanel Pin-header

Reference Designator: J36

2.54mm Pitch Pin-header, THT, straight, 10 circuits with removed 8th pin

Description

This connector provides Line-Out, Microphone-In optional either of the HD-Audio Codec (ALC888S) or I2S Codec (WM8904). See more details in chapter **"Functional Exclusives and Shared Resources"**.

Interfaces used

Line-Out, Microphone-In of the Audio-Codec (HDA or I2S)

Connector drawing and contact-numbering scheme

Figure 27 Audio Frontpanel Pin-header – J36

Pinout matching Intel Inhouse Standard

https://www.intel.co.uk/content/www/uk/en/support/articles/000005512/boards-and-kits/desktop-boards.html

	Pin	Signal / Function	Pin Type	Signal Description
J36	1	MIC_L	Analog	Microphone left channel
	2	GND	GND	Power Ground for panel supply
	3	MIC_R	Analog	Microphone right channel
	4	PRESENCE#	IN	not used; 10kohm pull up to 3.3V
	5	LINE_R	Analog	line out right channel
	6	SENSE_MIC_RETURN	Analog	microphone jack detecktion
	7	SENSE_SEND	Analog	jack detection sence line
	8	KEY (nc)	Key	removed pin (key)
	9	LINE_L	Analog	line out right channel
	10	SENSE_LINE_RETURN	Analog	line out jack detection

4.19. CAN0 Connector

Reference Designator: J41

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 4 circuits

Description

The J41 connector provides CAN0 Interface of the SMARC module over MCP2562 CAN transceiver.

Interfaces used

CAN0 Interface of the SMARC module

Connector drawing and contact-numbering scheme

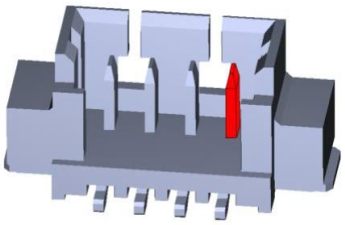


Figure 28 Connector – J41

Pinout according to Data Modul Inhouse-Standard DMIS10

	Pin	Signal / Function	Pin Type	Signal Description
J41	1	VCC	Power 5.0V (S0)	Power supply for attached device; max. current 200mA
	2	CAN_H	IO	High-level signal of the differential CAN
	3	CAN_L	IO	Low-level signal of the differential CAN datapair
	4	GND	GND	Connected to ground potential of the PCB

4.20. LVDS Display Connector

Reference Designator: J30

Hirose DF20 connector with 50 positions, unshielded, straight

Description

LVDS Display Connector supporting single or dual channel flat panels with graphics resolution up to FHD (1080p).

Interfaces used

LVDS0 and LVDS1 from SMARC module

VDD Display Power Supply

The VDD power supply is **default** connected to VCC 5.0V (S0) by R393 resistor.
To change VDD to 3.3V (S0) voltage, remove R393 and populate R394.

Connector drawing and contact-numbering scheme

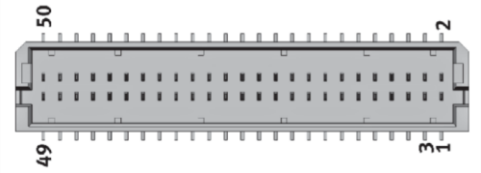


Figure 29 Connector – J30

Pinout according to Data Modul Inhouse-Standard DMIS01

	Pin	Signal / Function	Pin Type	Signal Description
J30	1	LVDS_GPIO1	IO (VDD)	LVDS 8/10bit Input Selection LOW: 8bit / HIGH: 10bit
	2	LVDS_GPIO2	IO (VDD)	LVDS Color Mapping LOW: JEIDA / HIGH: VESA
	3	LVDS_A0_N	O DP (LVDS)	LVDS Channel A (odd) pair 0, negative pin
	4	LVDS_B0_N	O DP (LVDS)	LVDS Channel B (even) pair 0, negative pin
	5	LVDS_A0_P	O DP (LVDS)	LVDS Channel A (odd) pair 0, positive pin
	6	LVDS_B0_P	O DP (LVDS)	LVDS Channel B (even) pair 0, positive pin
	7	GND	GND	Connected to ground potential of the PCB
	8	GND	GND	Connected to ground potential of the PCB
	9	LVDS_A1_N	O DP (LVDS)	LVDS Channel A (odd) pair 1, negative pin
	10	LVDS_B1_N	O DP (LVDS)	LVDS Channel B (even) pair 1, negative pin
	11	LVDS_A1_P	O DP (LVDS)	LVDS Channel A (odd) pair 1, positive pin
	12	LVDS_B1_P	O DP (LVDS)	LVDS Channel B (even) pair 1, positive pin
	13	GND	GND	Connected to ground potential of the PCB
	14	GND	GND	Connected to ground potential of the PCB
	15	LVDS_A2_N	O DP (LVDS)	LVDS Channel A (odd) pair 2, negative pin
	16	LVDS_B2_N	O DP (LVDS)	LVDS Channel B (even) pair 2, negative pin
	17	LVDS_A2_P	O DP (LVDS)	LVDS Channel A (odd) pair 2, positive pin
	18	LVDS_B2_P	O DP (LVDS)	LVDS Channel B (even) pair 2, positive pin

	Pin	Signal / Function	Pin Type	Signal Description
J30	19	GND	GND	Connected to ground potential of the PCB
	20	GND	GND	Connected to ground potential of the PCB
	21	LVDS_A_CLK_N	O DP (LVDS)	LVDS Channel A (odd) clk-pair, negative pin
	22	LVDS_B_CLK_N	O DP (LVDS)	LVDS Channel B (even) clk-pair, negative pin
	23	LVDS_A_CLK_P	O DP (LVDS)	LVDS Channel A (odd) clk-pair, positive pin
	24	LVDS_B_CLK_P	O DP (LVDS)	LVDS Channel B (even) clk-pair, positive pin
	25	GND	GND	Connected to ground potential of the PCB
	26	GND	GND	Connected to ground potential of the PCB
	27	LVDS_A3_N	O DP (LVDS)	LVDS Channel A (odd) pair 3, negative pin
	28	LVDS_B3_N	O DP (LVDS)	LVDS Channel B (even) pair 3, negative pin
	29	LVDS_A3_P	O DP (LVDS)	LVDS Channel A (odd) pair 3, positive pin
	30	LVDS_B3_P	O DP (LVDS)	LVDS Channel B (even) pair 3, positive pin
	31	GND	GND	Connected to ground potential of the PCB
	32	GND	GND	Connected to ground potential of the PCB
	33	Pulled to GND through a 10k-Ohms resistor	O DP (LVDS)	LVDS Channel A (odd) pair 4, negative pin
	34	Pulled to GND through a 10k-Ohms resistor	O DP (LVDS)	LVDS Channel B (even) pair 4, negative pin
	35	Pulled to GND through a 10k-Ohms resistor	O DP (LVDS)	LVDS Channel A (odd) pair 4, positive pin
	36	Pulled to GND through a 10k-Ohms resistor	O DP (LVDS)	LVDS Channel B (even) pair 4, positive pin
	37	LVDS_GPIO3	IO (VDD)	GPIO3, reserved for future use
	38	LVDS_GPIO4_ROTATE	IO (VDD)	Panel Rotation Display Control
				LOW: rotate disabled
				HIGH: rotate enabled
	39	LVDS_GPIO5_DIM	IO (VDD)	Local Dimming
				LOW: local dimming disabled
				HIGH: local dimming enabled
	40	LVDS_GPIO6_DDC-SDA	IO (VDD)	I2C data line
	41	V_VDD_LVDS_S0	Power (VDD)	Power-Supply for the panel; 3,3V or 5,0V
	42	LVDS_GPIO7_DDC-SCL	IO (VDD)	I2C clock line
	43	V_VDD_LVDS_S0	Power (VDD)	Power-Supply for the panel; 3,3V or 5,0V
	44	VDD_12V0_S0	Power (VDD12)	Power-Supply for the panel; 12,0V
	45	V_VDD_LVDS_S0	Power (VDD)	Power-Supply for the panel; 3,3V or 5,0V
	46	VDD_12V0_S0	Power (VDD12)	Power-Supply for the panel; 12,0V
	47	V_VDD_LVDS_S0	Power (VDD)	Power-Supply for the panel; 3,3V or 5,0V
	48	VDD_12V0_S0	Power (VDD12)	Power-Supply for the panel; 12,0V
	49	V_VDD_LVDS_S0	Power (VDD)	Power-Supply for the panel; 3,3V or 5,0V
	50	VDD_12V0_S0	Power (VDD12)	Power-Supply for the panel; 12,0V

4.21. V-By-One Display Connector

Reference Designator: J32

JAE FI-RE51S-HF connector with 51 positions, shielded, right-angled

Description

V-By-One connector supporting next generation flat panels with graphics resolution up to 4k (2160p).

Interfaces used

DP1 port from SMARC module over DisplayPort to Vx1 Bridge Novatek NT68410UBG.

Display Power Supply: V_TCON_5V_10V_12V can be selected through Jumper J60 between 5V/10V/12V.

The maximum current of 4.0A can be continuously sourced. Short overload up to 5A for Display test-mode is allowed.

The overcurrent protection is by set eFuse to 5.3A

Display Power Supply

The VDD (V-TCON) power supply is **default** selected to VCC 12.0V (S0) by J60.

Attention! The V-By-One panel-power can only be supplied either through the “V-By-One Displayconnector” J32 or the “V-By-One Display-Power-connector” J56

Connector drawing and contact-numbering scheme

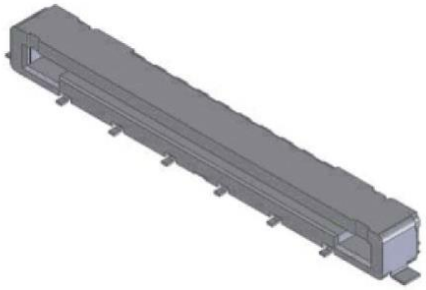


Figure 30 Connector – J32

Pinout according to Data Modul Inhouse-Standard DMIS12

	Pin	Signal / Function	Pin Type	Signal Description
J32	1	GND	GND	V-By-One HS CML ground
	2	VX1_TX7_P	O DP (CML)	V-By-One HS lane 7 (CML), positive pin
	3	VX1_TX7_N	O DP (CML)	V-By-One HS lane 7 (CML), negative pin
	4	GND	GND	V-By-One HS CML ground
	5	VX1_TX6_P	O DP (CML)	V-By-One HS lane 6 (CML), positive pin
	6	VX1_TX6_N	O DP (CML)	V-By-One HS lane 6 (CML), negative pin
	7	GND	GND	V-By-One HS CML ground
	8	VX1_TX5_P	O DP (CML)	V-By-One HS lane 5 (CML), positive pin
	9	VX1_TX5_N	O DP (CML)	V-By-One HS lane 5 (CML), negative pin
	10	GND	GND	V-By-One HS CML ground
	11	VX1_TX4_P	O DP (CML)	V-By-One HS lane (CML), positive pin
	12	VX1_TX4_N	O DP (CML)	V-By-One HS lane 4 (CML), negative pin
	13	GND	GND	V-By-One HS CML ground

	Pin	Signal / Function	Pin Type	Signal Description
J32	14	VX1_TX3_P	O DP (CML)	V-By-One HS lane 3 (CML), positive pin
	15	VX1_TX3_N	O DP (CML)	V-By-One HS lane 3 (CML), negative pin
	16	GND	GND	V-By-One HS CML ground
	17	VX1_TX2_P	O DP (CML)	V-By-One HS lane 2 (CML), positive pin
	18	VX1_TX2_N	O DP (CML)	V-By-One HS lane 2 (CML), negative pin
	19	GND	GND	V-By-One HS CML ground
	20	VX1_TX1_P	O DP (CML)	V-By-One HS lane 1 (CML), positive pin
	21	VX1_TX1_N	O DP (CML)	V-By-One HS lane 1 (CML), negative pin
	22	GND	GND	V-By-One HS CML ground
	23	VX1_TX0_P	O DP (CML)	V-By-One HS lane 0 (CML), positive pin
	24	VX1_TX0_N	O DP (CML)	V-By-One HS lane 0 (CML), negative pin
	25	GND	GND	V-By-One HS CML ground
	26	VX1_PLLLOCK#	IO (3.3V)	V-By-One HS lock detect
	27	VX1_HTPD#	IO (3.3V)	V-By-One HS hot plug detect
	28	OPTION_28 Tristate (default) GND (for AUO panels only)	IO/GND	User Option
	29	OPTION_29	IO (3.3V)	User Option
	30	OPTION_30	IO (3.3V)	User Option
	31	OPTION_31 Tristate (default) VX1_VSYNC (in)	IO (3.3V)	User Option
	32	OPTION_32	IO (3.3V)	User Option
	33	OPTION_33 Tristate (default) VX1_I2C_SCL	IO (3.3V)	User Option
	34	OPTION_34 Tristate (default) VX1_I2C_SDA	IO (3.3V)	User Option
	35	OPTION_35	IO (3.3V)	User Option
	36	OPTION_36	IO (3.3V)	User Option
	37	OPTION_37 / VX1_LD-EN Tristate (default) High (LD enabled) Low/GND (LD disabled)	IO (3.3V)	User option High (local dimming enabled) Low/GND (local dimming disabled)
	38	OPTION38 / GND	IO (3.3V)/GND	User Option or Power Ground for panel supply
	39	OPTION39 / GND	IO (3.3V)/GND	
	40	OPTION40 / GND	IO (3.3V)/GND	
	41	OPTION41 / GND	IO (3.3V)/GND	
	42	OPTION42 / GND	IO (3.3V)/GND	
	43	OPTION43	IO	GPIO

	Pin	Signal / Function	Pin Type	Signal Description
J32	44	OPTION44 / V_TCON_5V_10V_12V	IO (3.3V)/Power	Power-Supply for the panel; 5,0V, 10,0V or 12,0V
	45	OPTION45 / V_TCON_5V_10V_12V	IO (3.3V)/Power	User option or power-supply for the panel; 5,0V, 10,0V or 12,0V
	46	OPTION46 / V_TCON_5V_10V_12V	IO (3.3V)/Power	
	47	OPTION47 / V_TCON_5V_10V_12V	IO (3.3V)/Power	
	48	V_TCON_5V_10V_12V	Power	Power-Supply for the panel; 5,0V, 10,0V or 12,0V
	49	V_TCON_5V_10V_12V	Power	
	50	V_TCON_5V_10V_12V	Power	
	51	V_TCON_5V_10V_12V	Power	
	52	SHIELD	GND	Body-shield connections (10pcs) on SMT pins

4.22. V-By-One Display-Power-Connector (TCON)

Reference Designator: J56

2.50mm Pitch JST EH connector, wire-to-board header, THT, straight, 6 circuits

Description

Optional V-TCON power supply connector for Vx1 Display.

Interfaces used

Optional Vx1 Display Power Supply: V_TCON_5V_10V_12V can be selected through Jumper J60 between 5V/10V/12V.

The maximum current of 4.0A can be continuously sourced. Short overload up to 5A for Display test-mode is allowed.

The overcurrent protection is by set eFuse to 5.3A

Attention! The V-By-One panel-power can only be supplied either through the “V-By-One Display Connector” J56 or “V-By-One Display-Power-Connector” J32.

Connector drawing and contact-numbering scheme

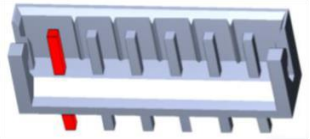


Figure 31 Connector – J56

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J56	1	GND	GND	Power ground for panel supply
	2	GND	GND	
	3	GND	GND	
	4	V_TCON_5V_10V_12V (5.0V, 10.0V or 12.0V)	Power	Power-supply for the panel; 5,0V, 10,0V or 12,0V
	5	V_TCON_5V_10V_12V (5.0V, 10.0V or 12.0V)	Power	
	6	V_TCON_5V_10V_12V (5.0V, 10.0V or 12.0V)	Power	

4.23. LVDS Display Backlight Connector

Reference Designator: J29

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 8 circuits

Description

Backlight power and control for LVDS display connected on J30 (DF20 Series) connector.

Interfaces used

LVDS Backlight control signals (Enable, PWM)
12V0 Power, max. current: 1.5 A
5V0 Power, max. current: 1.2 A

Connector drawing and contact-numbering scheme

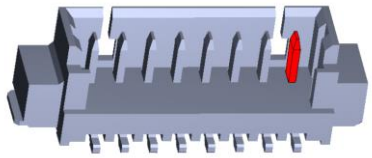


Figure 32 Connector – J29

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J29	1	V_12V0_S0	Power	12V supply voltage for the backlight, max 1.5A
	2	V_12V0_S0	Power	
	3	GND	GND	Connected to USB-ground potential of the PCB
	4	GND	GND	
	5	LVDS_BKLT_EN	O (3.3V) (optional 5V)	Backlight-Enable signal. Voltage-swing and polarity of this signal is implementation-dependent and designed as BOM-options
	6	LVDS_BKLT_CTRL	O (3.3V) (optional 5V)	PWM backlight-control signal. Voltage-swing and polarity of this signal is implementation-dependent and designed as BOM-options
	7	V_5V0_S0	Power	5V supply voltage for the backlight, max 1.2A
	8	V_5V0_S0	Power	

4.24. V-By-One Display Backlight Connector

Reference Designator: J33

2.50mm Pitch JST EH connector, wire-to-board header, THT, straight, 7 circuits

Description

Backlight power and control lines for V-By-One display.

Interfaces used

V-By-One Backlight Enable signal from the DP to V-By-One transmitter
V-By-One Backlight Control PWM signal from the DP to V-By-One transmitter
24V0 Power, max. current: 6.0A (3.0A per pin) Pinout

Connector drawing and contact-numbering scheme

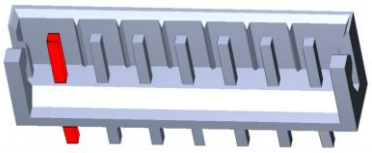


Figure 33 Connector – J33

Pinout according to Data Modul Inhouse-Standard DMIS13

	Pin	Signal / Function	Pin Type	Signal Description
J33	1	VBO_BKLT_ANADIM	O/Analog	Analog dimming control (max. 5V level)
	2	VBO_BKLT_PWMDIM	O (5V)	PWM backlight-control signal. Voltage-swing and polarity of this signal is implementation-dependent and designed as BOM-options
	3	VBO_BKLT_EN (TTL 5V)	O (5V)	Backlight-Enable signal. Voltage-swing and polarity of this signal is implementation-dependent and designed as BOM-options
	4	V_24V0_VBO_BKLT	Power	24V/max. 6A (not fused) backlight power.
	5	V_24V0_VBO_BKLT		
	6	GND	GND	Power Ground for panel supply
	7	GND		

4.25. System-Fan Connectors

Reference Designator: – J9, J10, J11, J12

2.54mm Pitch wire-to-board vertical header, with friction lock, 4 Circuits

Description

The eDM-CB-SM-IPCS provides four system fan connectors for thermal regulation.

TACHIN[0..3]: each of TACHIN signals is separately connected to the board controller. The board controller observing the rotation speed and forwarding the middle value of the all four TACHIN signal to the SMARC module.

PWM[0..3]: the SMARC PWM signal from module is 1:1 forwarded to each system fan. The rotation speed must be approximately equal if the same type of the system fan is used in design.

Interfaces used

FAN_PWMx output signal from the STM32 board controller

FAN_TACHINx input signal to the STM32 board controller

Connector drawing and contact-numbering scheme

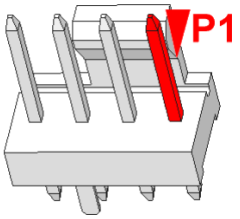


Figure 34 Connector – J9, J10, J11, J12

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J9 J10 J11 J12	1	Ground	GND	Fan ground
	2	V_12V0_S0_FAN	Power	12V fan power supply, max. current 150mA for each FAN
	3	FAN_TACHIN0x	I (1.8V - 5V)	Input for rotation counter
	4	FAN_PWMx output signal	O (5V)	PWM for fan-speed control (optional 3.3V)

4.26. DOOR Contact Connector

Reference Designator: – J8

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 2 circuits

Description

Door contact connector indicates via GPIO to board controller a case open event.

Interfaces used

GPIO pin of the STM32 board controller

Connector drawing and contact-numbering scheme

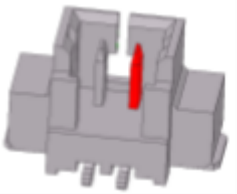


Figure 35 Connector – J8

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J8	1	Ground	GND	Connected to ground potential of the PCB
	2	DOOR_CONTACT	I (OD 3.3V)	Case open indication. 10k pull-up to 3.3V on CB.

4.27. Infrared-IF Connector

Reference Designator: – J3

1.27mm pitch Socket Strip, Top Entry SMT, 20 circuits

Description

The Infrared-IF connector provides Data Modul own developed Infrared Keyboard Interface.
The STM32 board controller converting the IR to USB HID Keyboard compatible device to SMARC.

Interfaces used

I2C-SW bus of the STM32 board controller
KBD_RED, KBD_GREEN and KBD_ORANGE status signals of the STM32 board controller
INFRARED_IN signal to the STM32 board controller
Power 5.0V (S5); max. current: 250 mA

Connector drawing and contact-numbering scheme

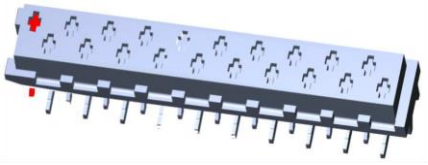


Figure 36 Connector – J3

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J3	1	GND	GND	Connected to ground potential of the PCB
	2	NC	NC	Not connected
	3	KBD_LED_RED	O (3.3V)	LED Driver for status indication (max. 20mA)
	4	KBD_LED_GREEN	O (3.3V)	LED Driver for status indication (max. 20mA)
	5	NC	NC	Not connected
	6	KBD_LED_ORANGE	O (3.3V)	LED Driver for status indication (max. 20mA)
	7	GND	GND	Connected to ground potential of the PCB
	8	I2C-SW_SDA	IO (CMOS 3,3V)	I2C data line
	9	GND	GND	Connected to ground potential of the PCB
	10	I2C-SW_SCL	O (CMOS 3,3V)	I2C clock line
	11	GND	GND	Connected to ground potential of the PCB
	12	GND	GND	Connected to ground potential of the PCB
	13,14, 15,16, 17	NC	NC	Not connected
	18	GND	GND	Connected to ground potential of the PCB
	19	V_5V0_S5	Power	5.0V (S5) power supply for IR device (max.250mA)
	20	INFRARED_IN	I	Input from IR device

4.28. GBE0,1 Precision Time Protocol Extension Connector

Reference Designator: – J58

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 4 circuits

Description

IEEE 1588 trigger signal for hardware implementation of PTP (Precision Time Protocol)

Interfaces used

GBE0,1_SDP signal of SMARC module
Power V_3V3_GBE; Imax = 10mA

Connector drawing and contact-numbering scheme

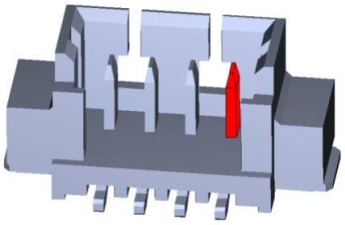


Figure 37 Connector – J58

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J58	1	V_3V3_GBE	GND	3.3V attached device power supply
	2	GBE0_SDP	IO (CMOS 3.3V)	GBE0 IEEE 1588 trigger signal for hardware implementation of PTP (Precision Time Protocol)
	3	GBE1_SDP	IO (CMOS 3.3V)	GBE1 IEEE 1588 trigger signal for hardware implementation of PTP (Precision Time Protocol)
	4	GND	GND	Connected to ground potential of the PCB

4.29. Data Modul Feature Connector

Reference Designator: – J51

1,27mm pitch dual-row SMT pin-header straight, 40 circuits

Description

The Data Modul feature connector covers minor system interfaces and status signals together with some power supply signals to provide an easy way for system designers to monitor the status of an embedded board, initiate different events and receive support for the system development process.

Interfaces used

SMARC control signals
I2C General purpose (GP) and power management (PM) bus
UART from carrier-board-board controller STM32 (for internal use only)
SMARC GPIOs [0..7]

Connector drawing and contact-numbering scheme

Figure 38 Connector – J51

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J51	1	GND	GND	Connected to ground potential of the PCB
	2	V_5V0_S0	Power	5.0V (S0) power supply for attached device (max.500mA)
	3	VIN_PWR_BAD#	O (OD, 1.8 - 5V)	Power bad indication from CB. Module and CB power supplies shall not be enabled while this signal is held low by the CB. A pull-up must be implemented on the SMARC module. Driven by OD on CB
	4	PWRBTN#	I(OD, 3.3V)	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. Power button events can be generated and monitored through the feature connector. This signal is being de-bounced by the embedded board, tactive, min=25ms
	5	CB_RESET#	O (CMOS 3.3V)	Platform reset is a reset signal generated by the SMARC module.
	6	GND	GND	Connected to ground potential of the PCB
	7	CB_STBY#	O (CMOS 3.3V)	The SMARC module drives this signal low when the system is in a standby power state. The CB switches all S0 power rails off.

	Pin	Signal / Function	Pin Type	Signal Description
J51	8	RESET_KEY#	I (OD, 3.3V)	Reset button input. Active low request for the embedded board to reset and reboot. Reset button events can be generated and monitored through the feature connector. This signal is being de-bounced by the embedded board, tactive, in=25ms
	9	CB_PWR_ON	O (CMOS 3.3V)	Carrier board circuits (apart from power management and power path circuits) are not powered up until the module asserts the CARRIER_PWR_ON signal.
	10	SUS_CLK	O (CMOS 3.3V)	
	11	GND	GND	Connected to ground potential of the PCB
	12	V_5V0_S0	Power	3.3V (S0) power supply for attached device (max.250mA)
	13	WDTO#	O (CMOS 3.3V)	
	14	SLEEP#	I (OD 3.3V)	Sleep indicator from CB to SMARC module. May be sourced from user Sleep button. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the Module.
	15	THERM#	IO (OD, 3.3V)	Indicates over-temp situations at some point on the Embedded Board or within the embedded system. Therm# events can be generated and monitored through the feature connector.
	16	LID#	O (OD)	LID switch. Used by the ACPI operating system to detect an open or closed lid.
	17	NC	NC	not connected
	18	I2C_PM_ALERT#	IO (OD, 3.3V)	SMARC I2C_PM bus alert
	19	I2C_GP_SDA	IO (OD, 3.3V)	SMARC I2C (GP) bus data line
	20	I2C_GP_SCL	IO (OD, 3.3V)	SMARC I2C (GP) bus clock line
	21	I2C_PM_SDA	IO (OD, 3.3V)	SMARC I2C (PM) bus data line
	22	I2C_PM_SCL	IO (OD, 3.3V)	SMARC I2C (PM) bus clock line
	23	GND	GND	Connected to ground potential of the PCB
	24	V_RTCBAT	Power	Real-time clock circuit-power output. Nominally +3.0V +/- 20mV ripple. V_RTCBAT is supplied from the on board 3V DC-DC when the system is stanby powerded or from the RTC Battery when the system is not powered. Do not connect this signal to the battery without protection.
	25	GPIO0	IO (OD, 3.3V)	GPIO signal 0 from the SMARC embedded board. Default direction is input.
	26	GPIO1	IO (OD, 3.3V)	GPIO signal 1 from the SMARC embedded board. Default direction is input
	27	GPIO2	IO (OD, 3.3V)	GPIO signal 2 from the SMARC embedded board. Default direction is input
	28	GPIO3	IO (OD, 3.3V)	GPIO signal 3 from the SMARC embedded board. Default direction is input
	29	GPIO4 / HDA_RST#	IO (OD, 3.3V)	GPIO signal 4 from the SMARC embedded board. Default direction is output. GPIO4 is connected to HD-Audio Codec reset signal when HD-Audio Codec is present.

	Pin	Signal / Function	Pin Type	Signal Description
J51	30	GPIO5 / PWM_OUT	IO (OD, 3.3V)	GPIO signal 5 from the SMARC embedded board. Default direction is output. Alternate Function: PWM_OUT from board controller (not used)
	31	GPIO6 / TACH_IN	IO (OD, 3.3V)	GPIO signal 6 from the SMARC embedded board. Default direction is output. Alternate Function: FAN Tach-In from/to SMARC module.
	32	GPIO7	IO (OD, 3.3V)	GPIO signal 7 from the SMARC embedded board. Default direction is output.
	33	MCU_USART1_RXD	IO (OD, 3.3V)	Serial data input to UART of the board controller STM32. Pull-up 47kOhm is present on CB. Internal use only.
	34	MCU_USART1_TXD	IO (OD, 3.3V)	Serial data output from UART of the board controller. Internal use only.
	35	NC	NC	not connected
	36	NC	NC	not connected
	37	NC	NC	not connected
	38	NC	NC	not connected
	39	NC	NC	not connected
	40	NC	NC	not connected

4.30. Piezo-Speaker (Buzzer)

Reference Designator: – LS1

Description

The carrier board provides integrated Piezo Speaker, sound output at 10 cm: min. 85 dB

Interface used

GPIO3 of the SMARC module
Supplied by 5,0 V S0 voltage (V_5V0_S0)

Connector drawing and contact-numbering scheme

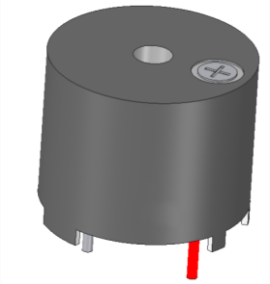


Figure 39 Piezo-Speaker – LS1

4.31. RTC-Battery Internal Connector

Reference Designator: – J54

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 2 circuits

Description

J54 is external RTC-Battery connection terminal with double protection against overcurrent and reversed polarity by diode and resistor in serial. The external RTC-Battery can be connected parallel to the on board CR2023 coin cell (J55).

Connector drawing and contact-numbering scheme

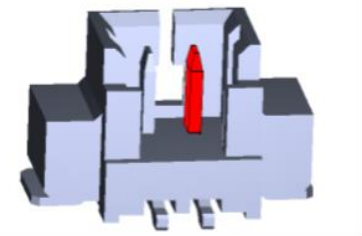


Figure 40 Connector – J54

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J54	1	V_3V0_BATCONN	Power	Coin cell positive (+) pole
	2	GND	GND	Coin cell negative (-) pole

4.32. RTC-Battery CR2023 Socket

Reference Designator: – J55

Description

The J55 is a RTC-Battery CR2023 socket. The RTC-Battery is protected against overcurrent and reversed polarity by diode and resistor in serial. The external RTC-Battery can be connected parallel to the on board CR2023 coin cell (J54).

Connector drawing and contact-numbering scheme

Figure 41 Connector – J55

4.33. System-I2C Connectors

Reference Designator: – J6/J7

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 2 circuits

Description

J6/J7 connectors provide I2C_SW bus of the eDM-CB-SM-IPCS board controller STM32 (U1) for internal slave devices.

Interface used

I2C-SW bus of the STM32 board controller
Power V_3V3_S5; Imax = 10mA

Connector drawing and contact-numbering scheme

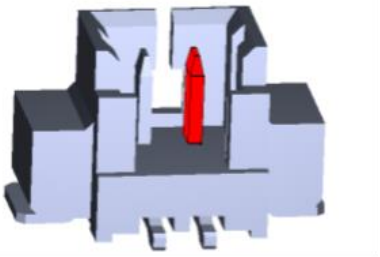


Figure 42 Connector – J6/J7

Pinout according to Data Modul Inhouse-Standard DMIS14

	Pin	Signal / Function	Pin Type	Signal Description
J6, J7	1	GND	GND	Connected to ground potential of the PCB
	2	I2C-SW_SCL	IO (CMOS 3.3V)	I2C clock line
	3	I2C-SW_SDA	IO (CMOS 3.3V)	I2C data line
	4	V_3V3_S5	Power 3.3V (S5)	Power supply for attached device; max. current 10mA

4.34. System-I2C 5V Connectors

Reference Designator: – J4/J5

1.25mm Pitch Molex PicoBlade wire-to-board header, SMT, straight, 4 circuits

Description

J4/J5 connectors provide I2C_SW **(CMOS 5V)** bus of the eDM-CB-SM-IPCS board controller STM32 (U1) for internal slave devices.

Interface used

I2C-SW bus of the STM32 board controller
Power V_5V0_S5; Imax = 10mA (each connector).

Connector drawing and contact-numbering scheme

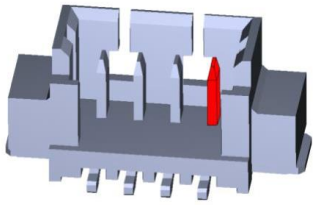


Figure 43 Connector – J4/J5

Pinout according to Data Modul Inhouse-Standard DMIS14

	Pin	Signal / Function	Pin Type	Signal Description
J4, J5	1	GND	GND	Connected to ground potential of the PCB
	2	I2C-SW_SCL	IO (CMOS 5V)	I2C clock line
	3	I2C-SW_SDA	IO (CMOS 5V)	I2C data line
	4	V_5V0_S5	Power 5.0V (S5)	Power supply for attached device; max. current 10mA

4.35. External Power-Button Connector

Reference Designator: – J61

1.25mm Pitch Molex PicoBlade Wire-to-board header, SMT, straight, 2 circuits

Description

J61 is an External Power-Button Terminal, which is connected parallel to the SW1 Button. The PWRBTN_KEY# is an open-drain signal to a General purpose input of the STM32 board controller. The board controller forwards the signal de-bounced by the uC firmware to the SMARC module.

Interfaces used

GPIO pin of the STM32 board controller

Connector drawing and contact-numbering scheme

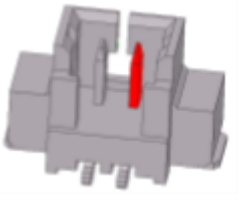


Figure 44 Connector – J61

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J61	1	PWRBTN_KEY#	I (OD 3.3V)	Power-Button Input to uC. 499kOhm pull-up to 3.3V on CB.
	2	Ground	GND	Connected to ground potential of the PCB

5. Jumpers, Switches and Status LEDs

5.1. Boot-Select Jumper

Reference Designator: – J44

Description

The carrier board provides array of 4 jumper-positions connected to FORCE_RECOV# and the BOOT_SEL[0:2]# signals of the SMARC module to allow any boot-device defined by the SMARC specification using a 8-pin header 2,54mm pitch THT

Component drawing and function table

Signal Name	Direction	Type / Tolerance	Description
BOOT_SEL[0:2]#	Input	CMOS 1.8V	Input straps determine the Module boot device. Pulled up on Module. Driven by OD part on Carrier.
FORCE_RECOV#	Input	CMOS 1.8V	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. Pulled high on the Module. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal ***may*** be used to load BIOS defaults. Pulled up on Module. Driven by OD part on Carrier.

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI (CS0#)
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

Figure 45 Connector – J44

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J44	1	FORCE_RECOV#	I (1.8V)	Boot-Strap Input
	2	GND	GND	Connected to ground potential of the PCB
	3	BOOT_SEL0#	I (1.8V)	Boot-Strap Input
	4	GND	GND	Connected to ground potential of the PCB
	5	BOOT_SEL1#	I (1.8V)	Boot-Strap Input
	6	GND	GND	Connected to ground potential of the PCB
	7	BOOT_SEL2#	I (1.8V)	Boot-Strap Input
	8	GND	GND	Connected to ground potential of the PCB

5.2. V-TCON Selection Jumper

Reference Designator: – J60

Description

The J60 voltage selection jumper allows selecting the V-TCON voltage level for V-By-One display between 5V/10V/12V.

Component drawing

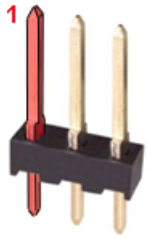


Figure 46 Connector – J60

Pinout

	Pin	Signal / Function	Pin Type	Signal Description
J60	1	V_TCON_12V	I	V-TCON 12V selection input, high active Pull-down 10kOhm on CB
	2	V_3V3_S0	Power 3.3V (S0)	Power for selektion pins
	3	V_TCON_10V	I	V-TCON 10V selection input, high active Pull-down 10kOhm on CB

Functional table. See voltage selection information printed on the PCB-Silkscreen below the J60.

V_TCON	V_TCON_10V	V_TCON_12V
5V	0	0
10V	1	0
12V	0	1
Force V-TCON DCDC enable override (V-TCON disabled)	1	1

5.3. Power-Button

Reference Designator: – SW1

Description

SW1 Power-Button is an open-drain driver to a General purpose input of the STM32 board controller.
The board controller forwards the signal de-bounced by the uC firmware to the SMARC module.
The SW1 is a SMT pushbutton switch with tactile feedback.
An external Power-Button can be connected to the 2-pin PicoBlade connector J61, which is connected parallel to the SW1.

Component drawing

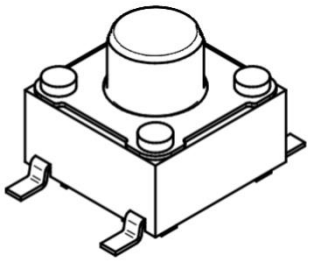


Figure 47 Power Button – SW1

5.4. Reset-Button

Reference Designator: – SW2

Description

SW2 Reset-Button is an open-drain driver to a General purpose input of the STM32 board controller.
The board controller forwarding by the uC-firmware de-bounced signal to the SMARC module.
The SW2 is a SMT pushbutton switch with tactile feedback.

Component drawing

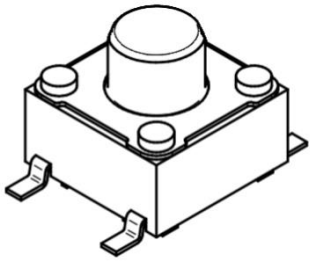


Figure 48 Power Button – SW2

5.5. System-State Status LEDs

RefDes	PCB Silkscreen Marking	Color	Signal / Function	Signal Description
D62	3V3 (STBY)	red	CB_STBY_3V3# (SUS_S3#)	LED active when SMARC module is NOT in S0 state
D57	CBON	green	CB_PWR_ON_3V3 (SUS_S5#)	LED active when SMARC carrier-board is powered on
D64	PGS5	green	PG_V_S5	LED active when all voltages of S5 power domain are active and within their specified range
D65	PGS0	green	PG_V_S0	LED active when all voltages of S0 power domain are active and within their specified range
D66	VVBO	green	PG_V_VBO	LED active when all voltages of the V-by-One function-block are active and within their specified range

*Note D62: there is an error in the printed PCB silkscreen information of D62. The marking will be corrected to **"STBY"** in the next PCB revision.*

5.6. M.2 and SATA-Activity LEDs

RefDes	PCB Silkscreen Marking	Color	Signal / Function	Signal Description
D10	M2A	red	LED_1# of M.2 Key-A	Depending on used M.2 card
D11	M2B	red	LED_1# of M.2 Key-B	Depending on used M.2 card
D81	SAct	red	SMARC_SATA_ACT#	LED blinks on activity at the SATA interface

5.7. USB Type-C Status LEDs

RefDes	PCB Silkscreen Marking	Color	Signal / Function	Signal Description
D73	TC_5V	green	USBC_PDO0	LED active when the USB Type-C connector-voltage is 5.0V
D72	TC_9V	green	USBC_PDO1	LED active when the USB Type-C connector-voltage is 9.0V
D75	TC_15V	green	USBC_PDO2	LED active when the USB Type-C connector-voltage is 15.0V
D74	TC_20V	green	USBC_PDO3	LED active when the USB Type-C connector-voltage is 20.0V
D76	TC_CTL1	green	USBC_MUX_CTL1	LED active when CTL1 pin of the USB Type-C port multiplexer is high; Refer to configuration-scheme according to chapter "USB Type-C Port Controller"
D77	TC_FLP	green	USBC_MUX_FLIP	LED active when the USB Type-C controller detects a device plugged in flipped mode. Refer to configuration-scheme according to chapter "USB Type-C Port Controller"
D78	TC_TCL0	green	USBC_MUX_CTL0	LED active when CTL0 pin of the USB Type-C port multiplexer is high; Refer to configuration-scheme according to chapter "USB Type-C Port Controller"

5.8. USB Type-C Multiplexing Scheme

CTL1-LED	CTL0-LED	FLIP-LED	USB Type-C Configuraiton	VESA DisplayPort ALT Mode DFP_D Configuraiotn
off	off	off	Power Downd	--
off	off	**ON**	Power Downd	--
off	**ON**	off	One Port USB3.1 - No Flip	--
off	**ON**	**ON**	One Port USB3.1 - Flip	--
ON	off	off	4 Lane DP - No Flip	C and E
ON	off	**ON**	4 Lane DP - Flip	C and E
ON	**ON**	off	One Port USB3.1 + 2 Lane DP - No Flip	D and F
ON	**ON**	**ON**	One Port USB3.1 + 2 Lane DP - Flip	D and F

6. Functional Exclusives and Shared Resources

6.1. DisplayPort (DP1) Sharing

The **DP1 DisplayPort** of the SMARC module is shared by following features:

- **V-By-One** transmitter which providing V-By-One Interface on **J32**
- **USB Type-C** connector **J26** at the I/O shield, to support DP-alternate mode

Note: It is not possible to use both features at the same time.

DP1 Port Switch Modification Instruction

To switch DP1 Port to V-By-One or to USB Type-C see the **"DP1 Shared Components Modification Table"** below. Use **"D001_AssemblyDrawing_eDM-CB-SM-IPCS.pdf"** to locate components on the PCB.

RefDes	V-By-One	USB Type-C Alternate Mode	Component Parameters
C187	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
C188	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
C191	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
C192	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
C195	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
C196	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
C199	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
C200	Add	Remove	100nF capacitor MLCC / X5R / 0201 package
R1052	Add	Remove	0 Ohm resistor / 0201 package
R1053	Add	Remove	0 Ohm resistor / 0201 package
R362	Add	Remove	0 Ohm resistor / 0201 package
C189	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C190	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C193	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C194	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C197	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C198	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C201	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C202	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
R1054	Remove	Add	0 Ohm resistor / 0201 package
R1055	Remove	Add	0 Ohm resistor / 0201 package
R363	Remove	Add	0 Ohm resistor / 0201 package

6.2. USB3.0 (Port 2) Sharing

The **USB3.0 Port 2** of the SMARC module is shared by following features:

- **USB3.0 Upper Port** of the **J24** - Dual USB 2.0 Type-A connector at the I/O shield
- **USB Type-C** connector **J26** at the I/O shield

Note: It is not possible to use both features at the same time.

USB3.0 Port 2 Switch-Modification Instruction

To switch the USB3.0 Port 2 to J24 or to J26 see the **"USB3.0-P2 Shared Components Modification Table"** below.

Use **"D001_AssemblyDrawing_eDM-CB-SM-IPCS.pdf"** to locate components on the PCB.

RefDes	USB3.0 Type-A J24 (upper port)	USB Type-C J26	Component Parameters
R253	Add	Remove	0 Ohm resistor / 0201 package
R254	Add	Remove	0 Ohm resistor / 0201 package
R257	Add	Remove	0 Ohm resistor / 0201 package
R258	Add	Remove	0 Ohm resistor / 0201 package
C607	Add	Remove	0 Ohm resistor / 0201 package (see Note C*)
C606	Add	Remove	0 Ohm resistor / 0201 package (see Note C*)
C571	Add	Remove	0 Ohm resistor / 0201 package (see Note C*)
C572	Add	Remove	0 Ohm resistor / 0201 package (see Note C*)
R265	Add	Remove	0 Ohm resistor / 0201 package
R255	Remove	Add	0 Ohm resistor / 0201 package
R256	Remove	Add	0 Ohm resistor / 0201 package
R259	Remove	Add	0 Ohm resistor / 0201 package
R260	Remove	Add	0 Ohm resistor / 0201 package
C604	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
C605	Remove	Add	100nF capacitor MLCC / X5R / 0201 package
R266	Remove	Add	0 Ohm resistor / 0201 package

*Note C *: This component is really a resistor, despite the use of the REfDes prefix "C" for this component*

Table 1 USB3.0-P2 Shared Components Modification Table

6.3. USB2.0 (Port 1B) Sharing

The **USB2.0 Port 1B** of the on board USB2.0 Hub is shared by following features:

- USB2.0 Upper port of the **J22** - Dual USB 2.0 Type-A connector at the I/O shield
- USB2.0 (Port 0) of the internal Pin-header **J21**

Note: It is not possible to use both features at the same time.

USB2.0 Port 1B Switch Modification Instruction

To switch USB2.0 Port 1B to J21or J22 connector see the **"USB2.0-P1B Shared Components Modification Table"** below. Use **"D001_AssemblyDrawing_eDM-CB-SM-IPCS.pdf"** to locate components on the PCB.

RefDes	USB2.0 Pinheader J21 (Port 0)	USB2.0 Type-A J22 (Upper Port)	Component Parameters
R231	Add	Remove	0 Ohm resistor / 0201 package
R232	Add	Remove	0 Ohm resistor / 0201 package
R233	Remove	Add	0 Ohm resistor / 0201 package
R234	Remove	Add	0 Ohm resistor / 0201 package

6.4. Audio (Line Out) J37 Shared Sources

The Audio line out of the J37 connector at the IO-Shield can be shared between following sources:

- Line Out of the I2S Audio Codec WM8904
- Front Line Out of the HD-Audio Codec ALC888S

Note: It is not possible to use both sources at the same time.

Audio line out Switch Modification Instruction

To switch Audio line out of the J37 between I2S or HD-Audio Codec see the **"Line-Out J37 Shared Components Modification Table"** below. Use **"D001_AssemblyDrawing_eDM-CB-SM-IPCS.pdf"** to locate components on the PCB.

RefDes	I2S Codec	HD-Audio Codec	Component Parameters
C320	Add	Remove	4.7uF capacitor MLCC / X5R / 0402 package
C321	Add	Remove	4.7uF capacitor MLCC / X5R / 0402 package
R490	Add	Remove	0 Ohm resistor / 0201 package
R491	Add	Remove	0 Ohm resistor / 0201 package
R506	Remove	Add	75 Ohm resistor / 0402 package
R507	Remove	Add	75 Ohm resistor / 0402 package
R492	Remove	Add	0 Ohm resistor / 0201 package
R495	Remove	Add	22.1 kOhm resistor / 0201 package
R496	Remove	Add	22.1 kOhm resistor / 0201 package
R493	Remove	Add	0 Ohm resistor / 0603 package

6.5. Audio (Internal Pin-header) J36 Shared Sources

The Audio line out and Microphone Input of the J36 Internal Pin-header can be shared between following sources:

- HP Out and Microphone of the I2S Audio Codec WM8904
- Line Out and Microphone of the HD-Audio Codec ALC888S

Note: It is not possible to use both sources at the same time.

Audio line out Switch Modification Instruction

To switch the audio lines of the J36 between I2S or HD-Audio Codec see the **"Audio Internal Pin-header J37 Shared Components Modification Table"** below. Use **"D001_AssemblyDrawing_eDM-CB-SM-IPCS.pdf"** to locate components on the PCB.

RefDes	I2S Codec	HD-Audio Codec	Component Parameters
C325	Add	Remove	10uF capacitor MLCC / X5R / 0603 package
C326	Add	Remove	10uF capacitor MLCC / X5R / 0603 package
C327	Add	Remove	10uF capacitor MLCC / X5R / 0603 package
C328	Add	Remove	10uF capacitor MLCC / X5R / 0603 package
R510	Add	Remove	0 Ohm resistor / 0603 package
R1069	Add	Remove	0 Ohm resistor / 0603 package
R502	Remove	Add	4.75 kOhm resistor / 0201 package
R503	Remove	Add	4.75 kOhm resistor / 0201 package
R504	Remove	Add	4.75 kOhm resistor / 0201 package
R505	Remove	Add	4.75 kOhm resistor / 0201 package
R497	Remove	Add	75 Ohm resistor / 0402 package
R498	Remove	Add	75 Ohm resistor / 0402 package
R499	Remove	Add	75 Ohm resistor / 0402 package
R500	Remove	Add	0 Ohm resistor / 0201 package
R501	Remove	Add	75 Ohm resistor / 0402 package
R509	Remove	Add	0 Ohm resistor / 0603 package
R1068	Remove	Add	0 Ohm resistor / 0603 package

6.6. I2S0 Interface Sharing

The I2S0 Interface of the SMARC module can be shared between following sources:

- I2S Audio Codec WM8904
- I2S Digital Microphone Connector J39

Note: It is not possible to use both sources at the same time.

I2S0 Interface Switch Modification Instruction

To switch the I2S0 Interface of the SMARC between I2S-Audio and J39 see the **"I2S0 Shared Components Modification Table"** below. Use **"D001_AssemblyDrawing_eDM-CB-SM-IPCS.pdf"** to locate components on the PCB.

RefDes	I2S Digital Microphone	I2S-Audio Codec	Component Parameters
R511	Add	Remove	0 Ohm resistor / 0201 package
R512	Add	Remove	0 Ohm resistor / 0201 package
R513	Add	Remove	0 Ohm resistor / 0201 package
R514	Remove	Add	0 Ohm resistor / 0201 package
R515	Remove	Add	0 Ohm resistor / 0201 package
R516	Remove	Add	0 Ohm resistor / 0201 package
R992	Remove	Add	0 Ohm resistor / 0201 package

6.7. SATA Interface Sharing

The SATA Interface of the SMARC module can be shared between following sources:

- SATA L-Shape Connector **J20**
- M.2 Key-M **J19**

Note: It is not possible to use both sources at the same time.

SATA Interface Switch Modification Instruction

To switch the SATA Interface of the SMARC between J20 or J19 see the **"SATA Shared Components Modification Table"** below. Use **"D001_AssemblyDrawing_eDM-CB-SM-IPCS.pdf"** to locate components on the PCB.

RefDes	SATA L-Shape (J20)	M.2 Key-M (J19)	Component Parameters
R201	Add	Remove	0 Ohm resistor / 0201 package
R202	Add	Remove	0 Ohm resistor / 0201 package
R205	Add	Remove	0 Ohm resistor / 0201 package
R206	Add	Remove	0 Ohm resistor / 0201 package
R203	Remove	Add	0 Ohm resistor / 0201 package
R204	Remove	Add	0 Ohm resistor / 0201 package
R207	Remove	Add	0 Ohm resistor / 0201 package
R208	Remove	Add	0 Ohm resistor / 0201 package

6.8. Power Supply to V-By-One Display (V-TCON)

The V-TCON Power Supply to the V-By-One display is provided on following connectors:

- **J32** – the 51-pin V-By-One combined data/power connector
- **J56** – the 6-pin separate V-By-One V-By-One Display-Power-connector

Attention!

The V-TCON maximum current is limited to 4A (5A for the short Dispay Test Mode).
Do not source the V-TCON power on both connectors at the same time!

6.9. I2C Devices

Four I2C Buses are available on the eDM-CB-SM-IPCS.

- I2C_GP: SMARC General purpose Interface
- I2C_PM: SMARC Power Management Support
- I2C_LCD: LSMARC LCD Display Support
- I2C_SW: STM32 board controller internal interface.

The I2C-Devices Table below shows the on board I2C device resources.

RefDes	Device	I2C Bus	I2C Addr.(8h)	Description
U1	Board Controller STM32	GP	52h	Connected to Ground potential of the PCB
U1	Board Controller STM32	PM	not used	reserved connection
U14	TPS65987D	GP	44h	USB-Type C Port Multiplexer
U25	WM8904	GP	34h	I2S Audio Codec
U31	AT24C32	GP	AEh	On Board EEPROM
U17	NT68410	LCD	A0h	Novatek DisplayPort to V-By-One Converter
U31	AT24C32	SW	A0h	EEPROM internal use only
U4	LM75	SW	92h	Temperature Sensor used by Board Controller STM32
U7	USB2514B	PM	58h	Optional connection to USB2.0- HUB

6.10. I2C Bus Topology

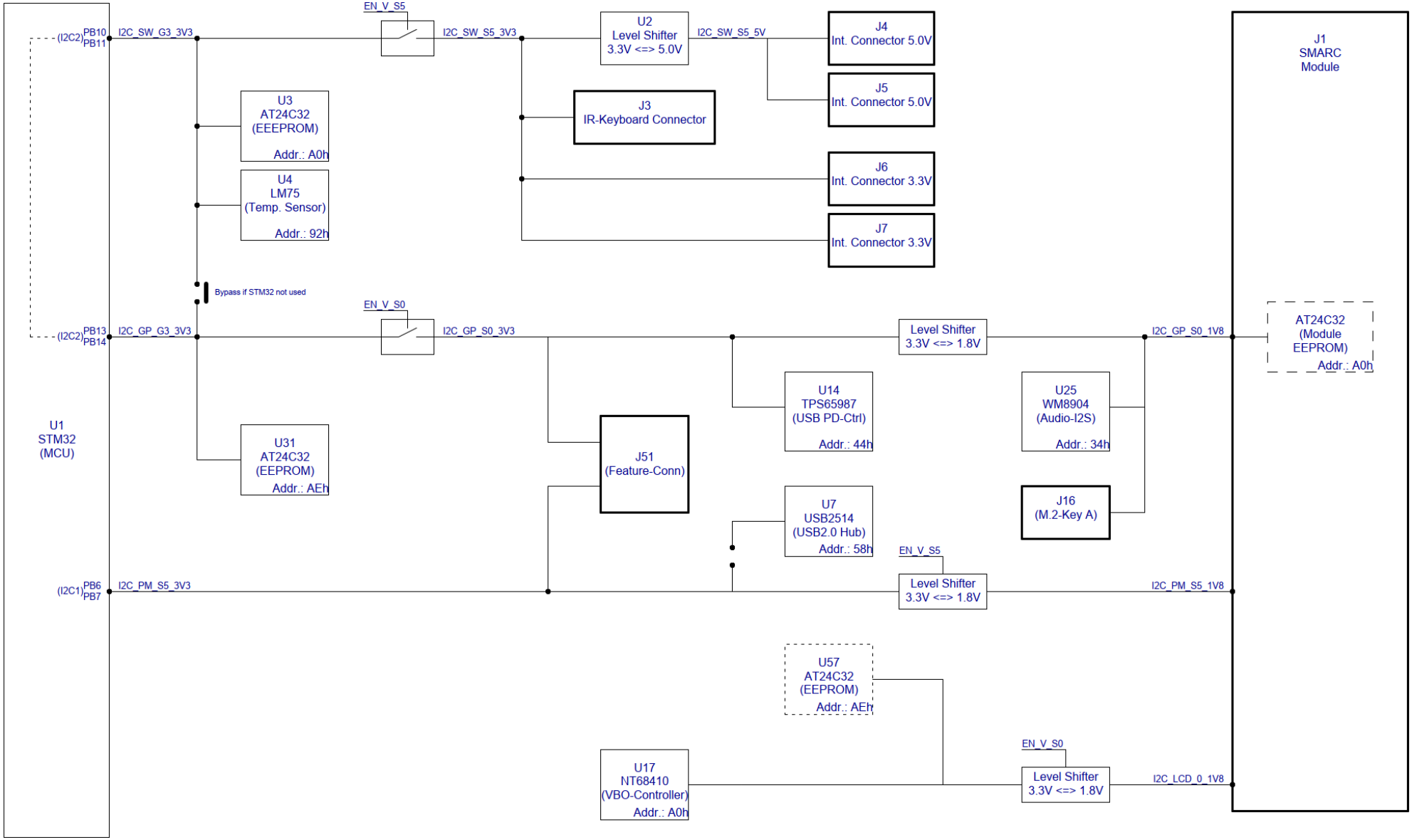


Figure 49 I2C-Bus Topology

7. Mechanical Design and EMI/ESD Shielding

7.1. PCB Size

Mechanical dimensions: 170,0 mm x 170,0 mm x 1,6 mm
According to Mini-ITX specification Figure 2 and Figure 3

7.2. Maximum component height

top side: 17,0 mm (Dual USB-A connector at I/O shield)
bottom side: 6,0 mm

7.3. Mounting Holes

The base plate is located at the bottom of the eDM-CB-SM-IPCS system. The eDM-CB-SM-IPCS with the SMARC module mounted on top of it rests on threaded standoffs located at the base plate matching mounting holes type “A” and “B”.

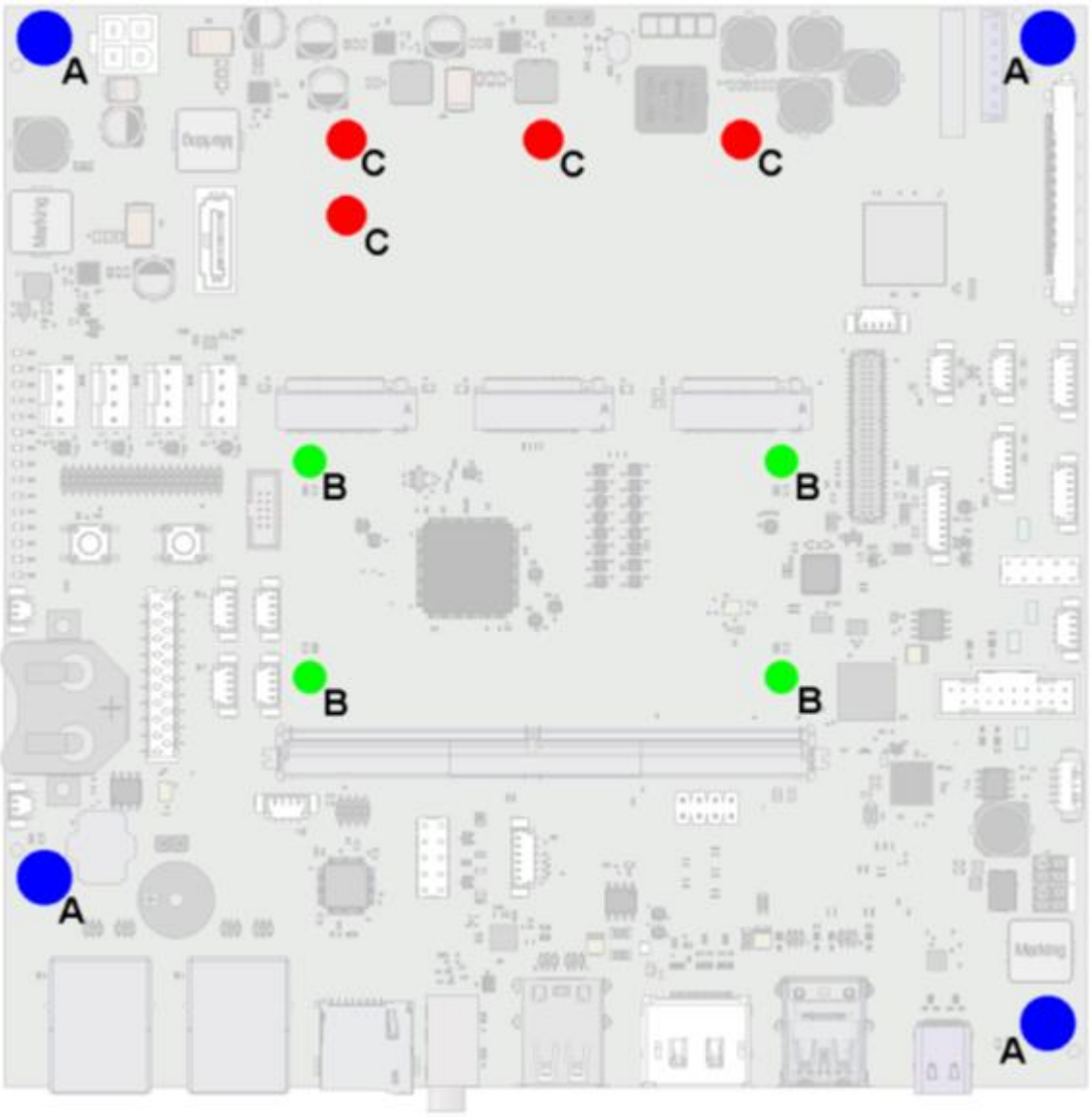


Figure 50 Mounting Holes

7.4. Mounting Concept

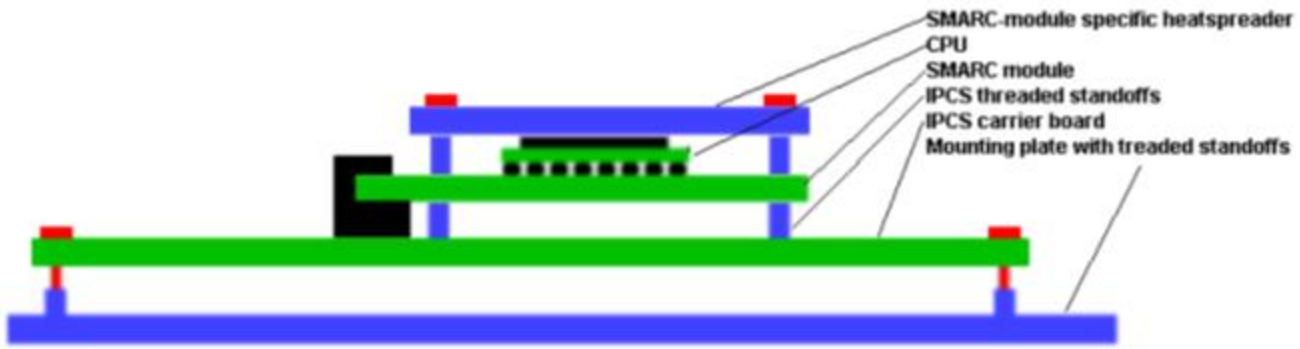


Figure 51 Mounting Concept

7.5. EMI and ESD-Shielding

The eDM-CB-SM-IPCS will be mounted on to a metal plate used as sink for electromagnetic interferences and unwanted charges.
The metal plate is connected as follows with the PCB.

	mechanical
A	**PCB ↔ mounting plate:** Carrier-Board mounting-holes with 8,4 mm pad and 3,2 mm drill diameter according to Mini-ITX specification Figure 3
B	**SMARC module ↔ PCB ↔ mounting plate:** SMARC module mounting-holes with 6,0 mm pad and 3,7 mm drill diameter to hold solder-in threaded M2.5 standoffs
C	**PCB only, no connection at mounting plate:** M.2 card-mounting positions with 7,4 mm pad and 4,4 mm drill diameter to hold solder-in threaded M3 standoffs

	electrical
A	Connect through a 100nF capacitor to PCB digital ground Direct connect to PCB chassis ground Direct connect to mounting plate through metal standoffs
B	Connect through zero ohm resistor to PCB digital ground No connection at mounting plate
C	Direct connect to PCB digital ground No connection at mounting plate Expect direct connection to M.2-card digital GND or unconnected contact area at M.2-card

Table 2 Mounting Points Description

Any shield or housing of a connector is directly connected to the PCB chassis ground.
Each interface connected to a cable connector is optionally protected against EMI with mating common mode chokes or ferrite beads, which could be stuffed if necessary.
Each external interface is protected against ESD via specific diodes.

For further discharge the eDM-CB-SM-IPCS chassis-GND nets are electrically connected through the mounting plate and metal standoffs to the PE (earth) contact of the building mains supply.

7.6. Mounting Holes - Mechanical Positions

All dimensions given are in millimeters [mm]

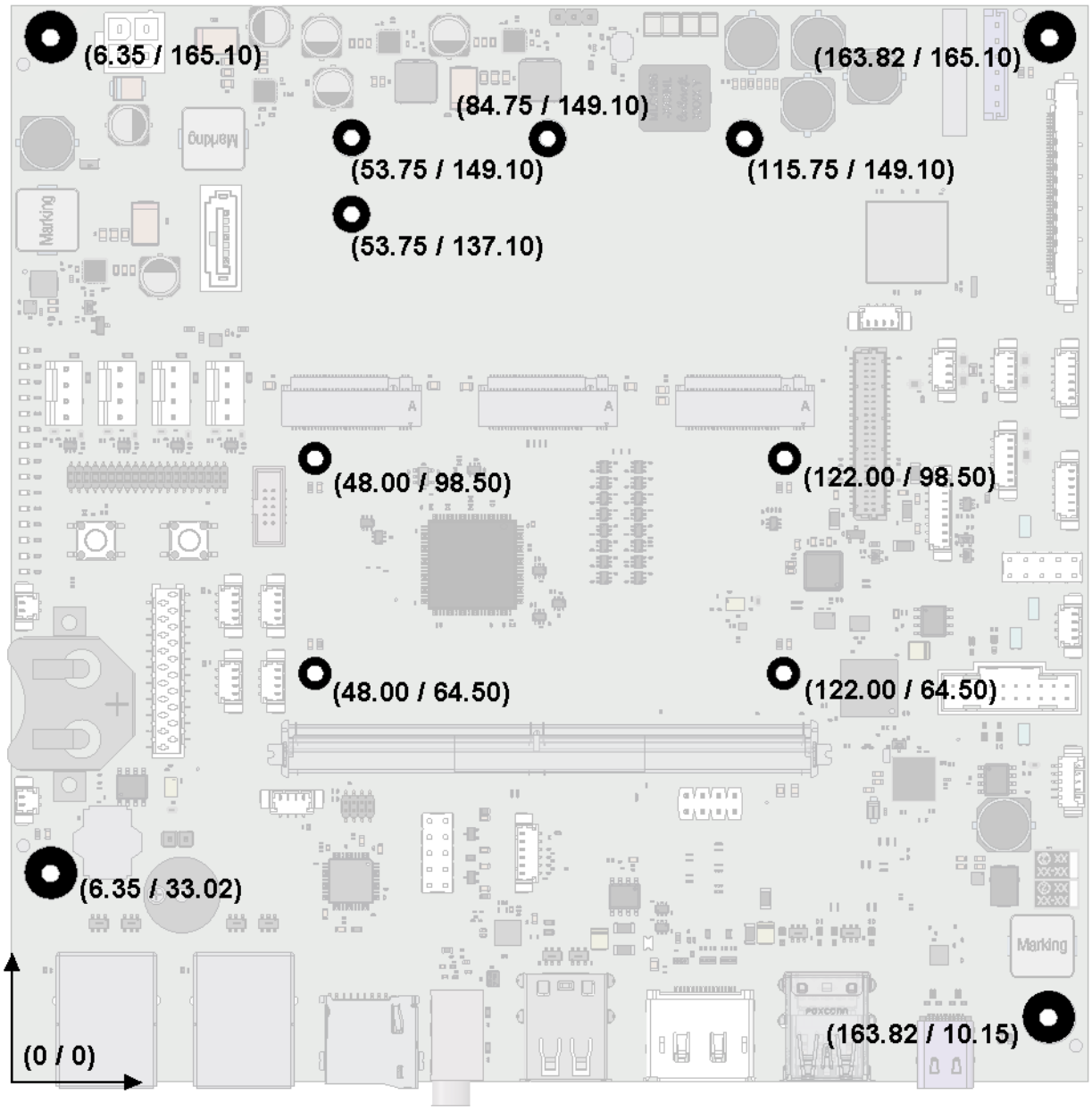
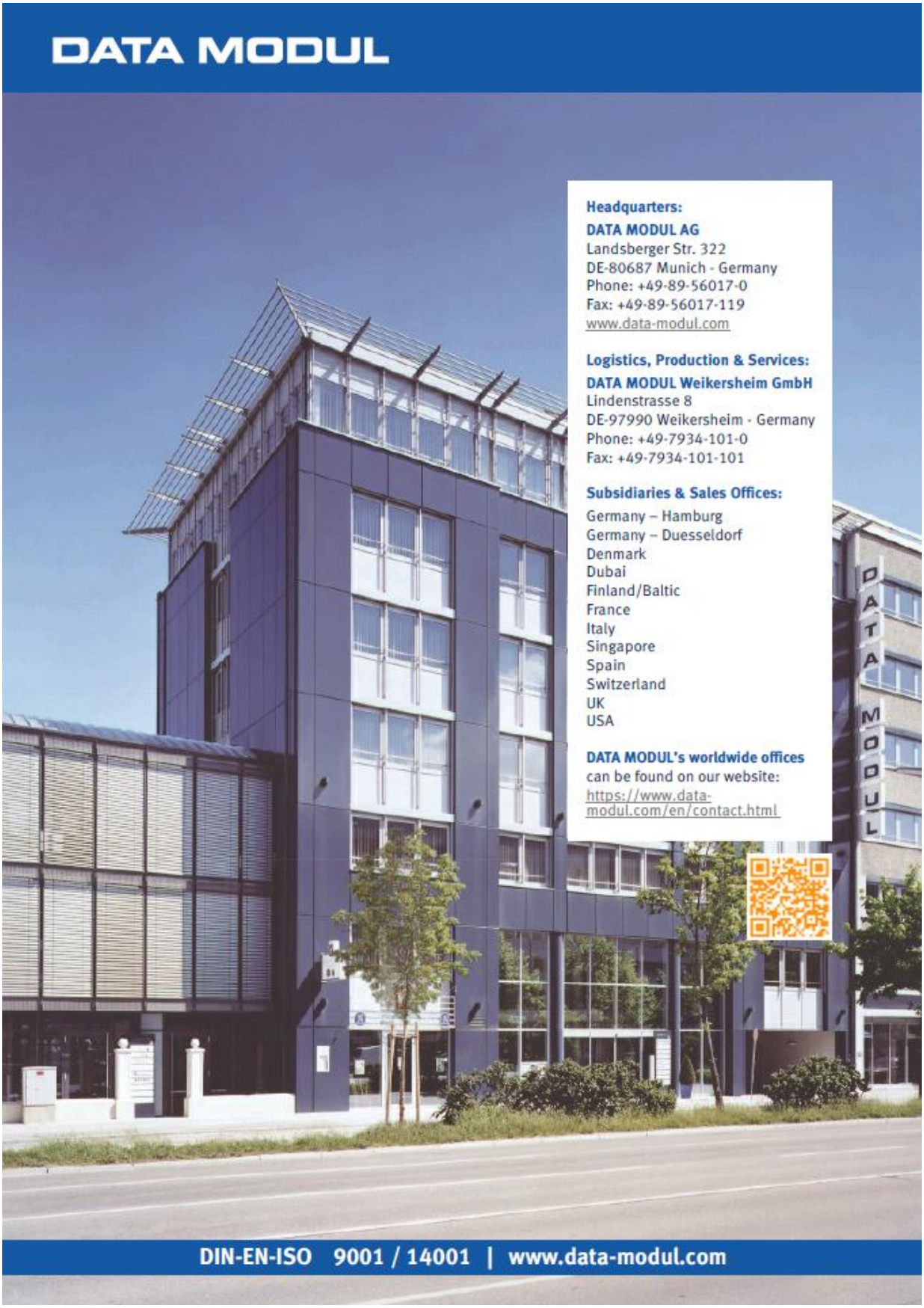


Figure 52 Mounting Holes - Mechanical Position


DATA MODUL
Headquarters:
DATA MODUL AG
Landsberger Str. 322
DE-80687 Munich - Germany
Phone: +49-89-56017-0
Fax: +49-89-56017-119
www.data-modul.com
Logistics, Production & Services:
DATA MODUL Weikersheim GmbH
Lindenstrasse 8
DE-97990 Weikersheim - Germany
Phone: +49-7934-101-0
Fax: +49-7934-101-101
Subsidiaries & Sales Offices:
Germany – Hamburg
Germany – Duesseldorf
Denmark
Dubai
Finland/Baltic
France
Italy
Singapore
Spain
Switzerland
UK
USA
DATA MODUL's worldwide offices
can be found on our website:
https://www.data-modul.com/en/contact.html
DATA MODUL
DIN-EN-ISO 9001 / 14001 | www.data-modul.com